

Code Name : Mink  
Project Name : Mink  
Version : A00  
Date : 2010/08/25

FLEXTRONICS CONFIDENTIAL

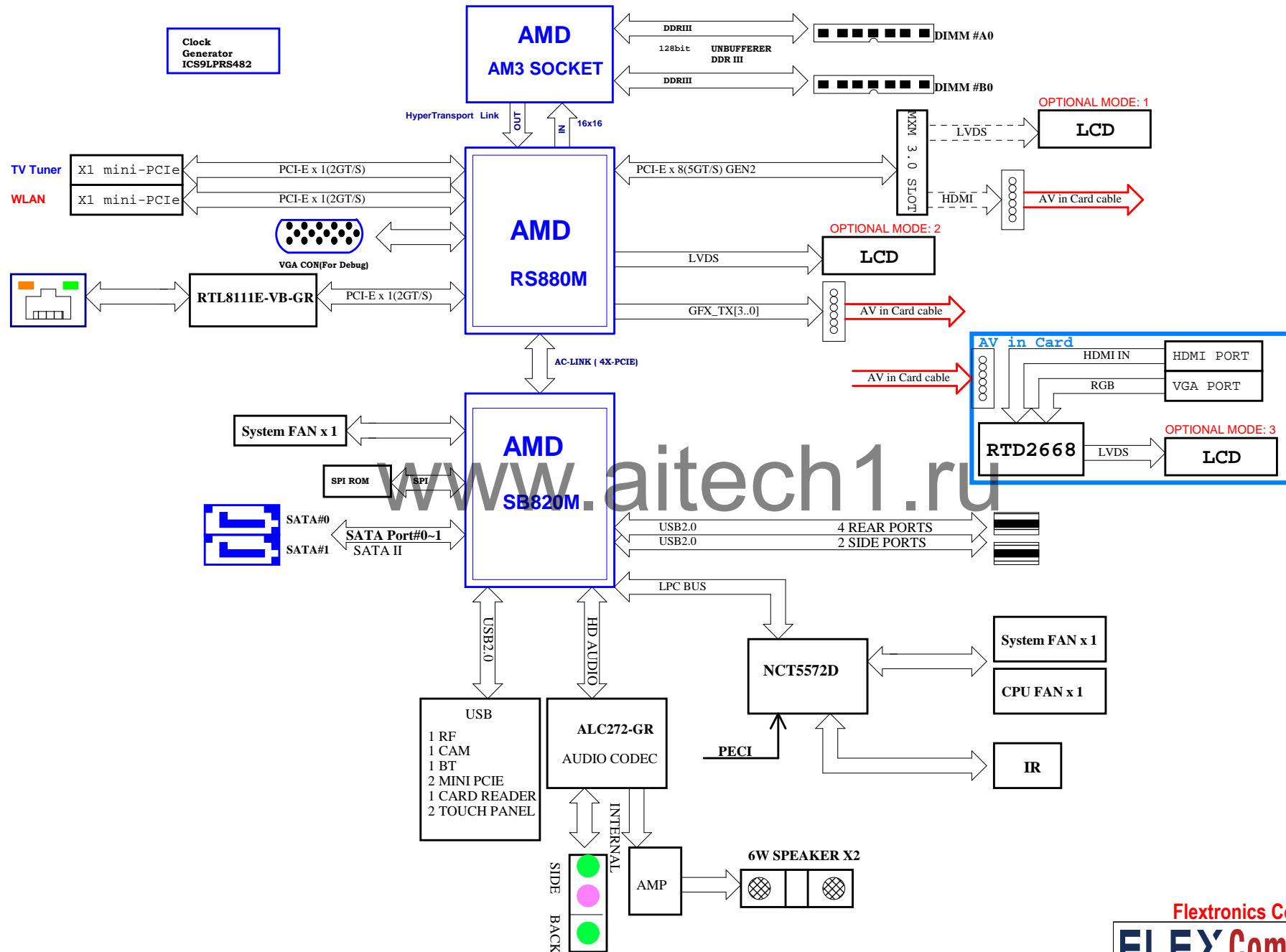
PCB SIZE :196.1mmx255mm  
PCB Thickness : 62 +8/-5 mils  
6 Layers

DO NOT DISTRIBUTE  
THESE SCHEMATICS ARE NOT VALIDATED

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30	AUDIO ALC272-GR

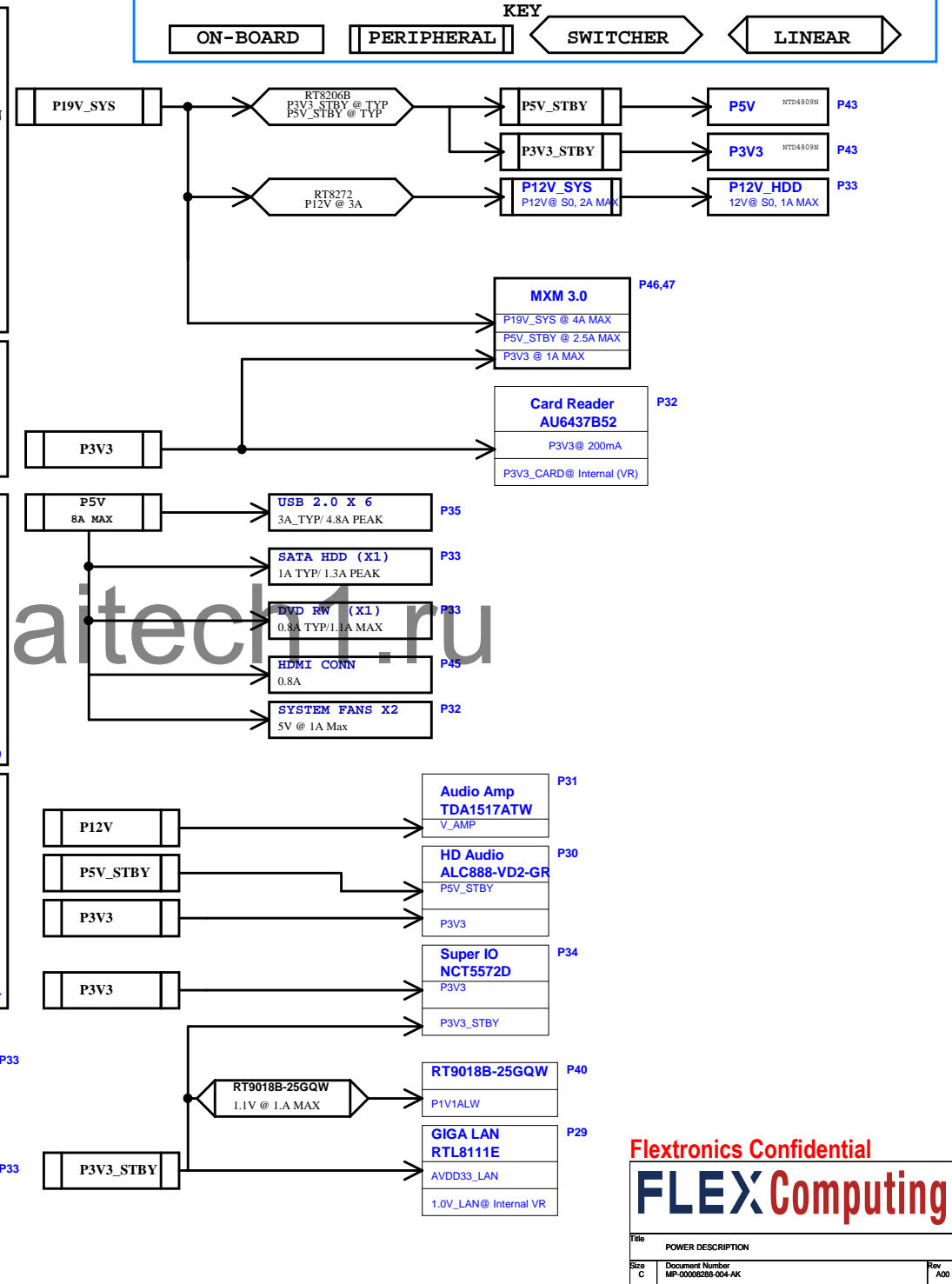
Page	Description
31	AMP & HP & SPDIF & L-Out
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37	CPU Core PWM
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# BLOCK DIAGRAM



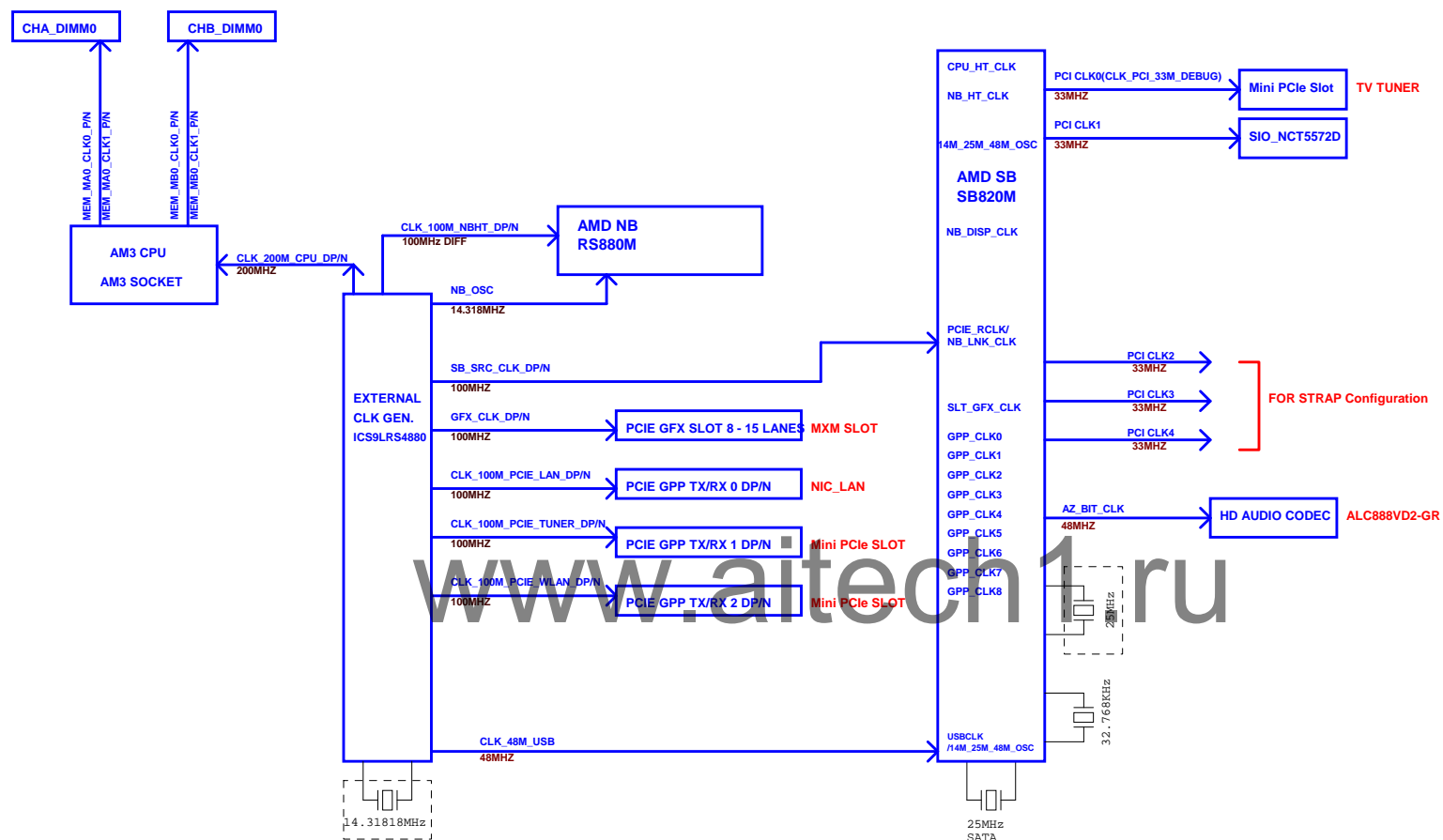
KEY

ON-BOARD PERIPHERAL SWITCHER LINEAR

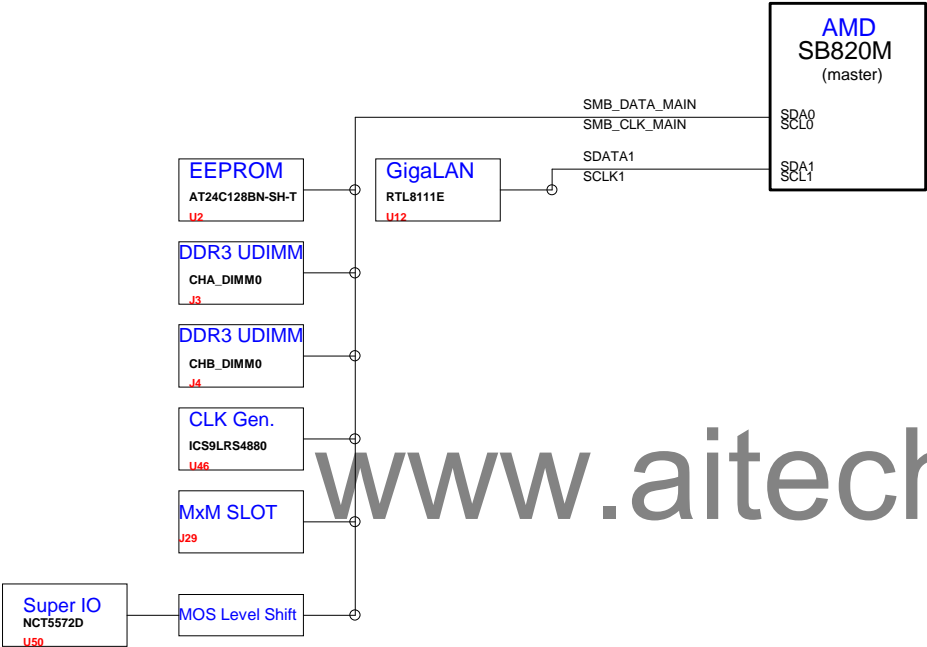


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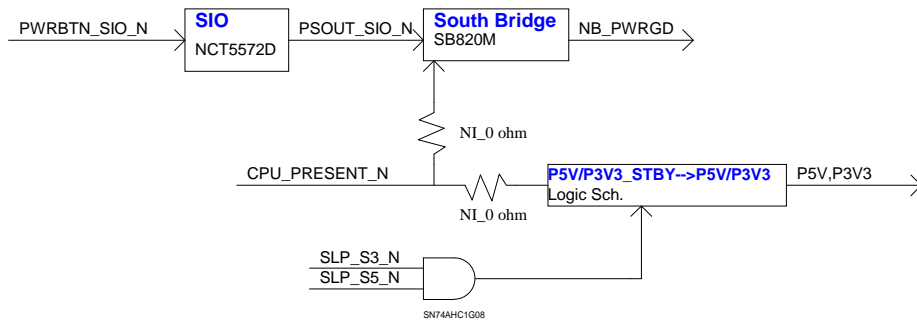
Title			
POWER DESCRIPTION			
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# SMBus Block Diagram

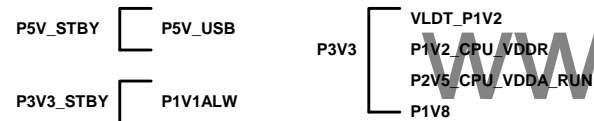


# POWER SEQUENCE DIAGRAM



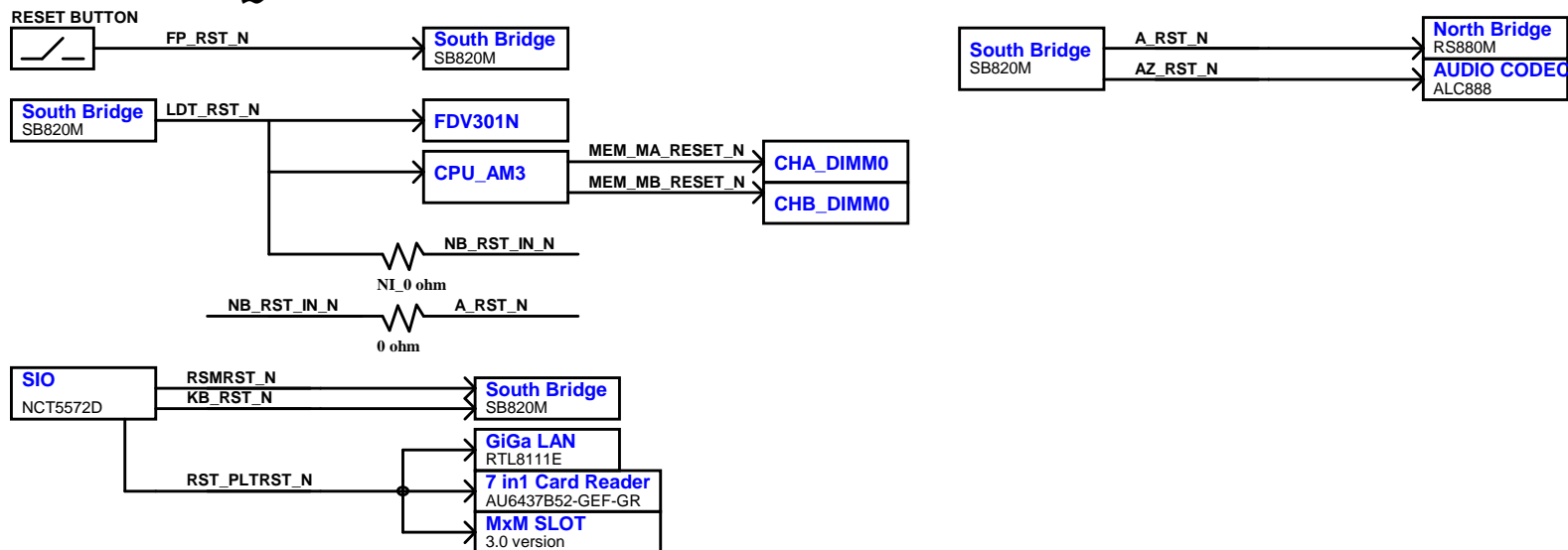
Power sequence : P19V\_SYS --> P5V\_STBY,P3V3\_STBY --> P5V,P3V3 --> P12V --> P1V5\_CPU\_VDDIO\_SUS --> P1V1 --> P1V25 --> P1V2\_CPU\_VDDNB\_RUN --> CPU\_VCORE --> VRM\_PWRGD --> SB\_PWRGD --> NB\_PWRGD\_IN

SLP\_S5\_N P19V\_SYS P5V\_STBY,P3V3\_STBY P5V,P3V3 P12V P1.5V\_CPU\_VDDIO\_SUS P1V1 P1V25 P1V2\_CPU\_VDDNB\_RUN CPU\_VCORE SB\_PWRGD

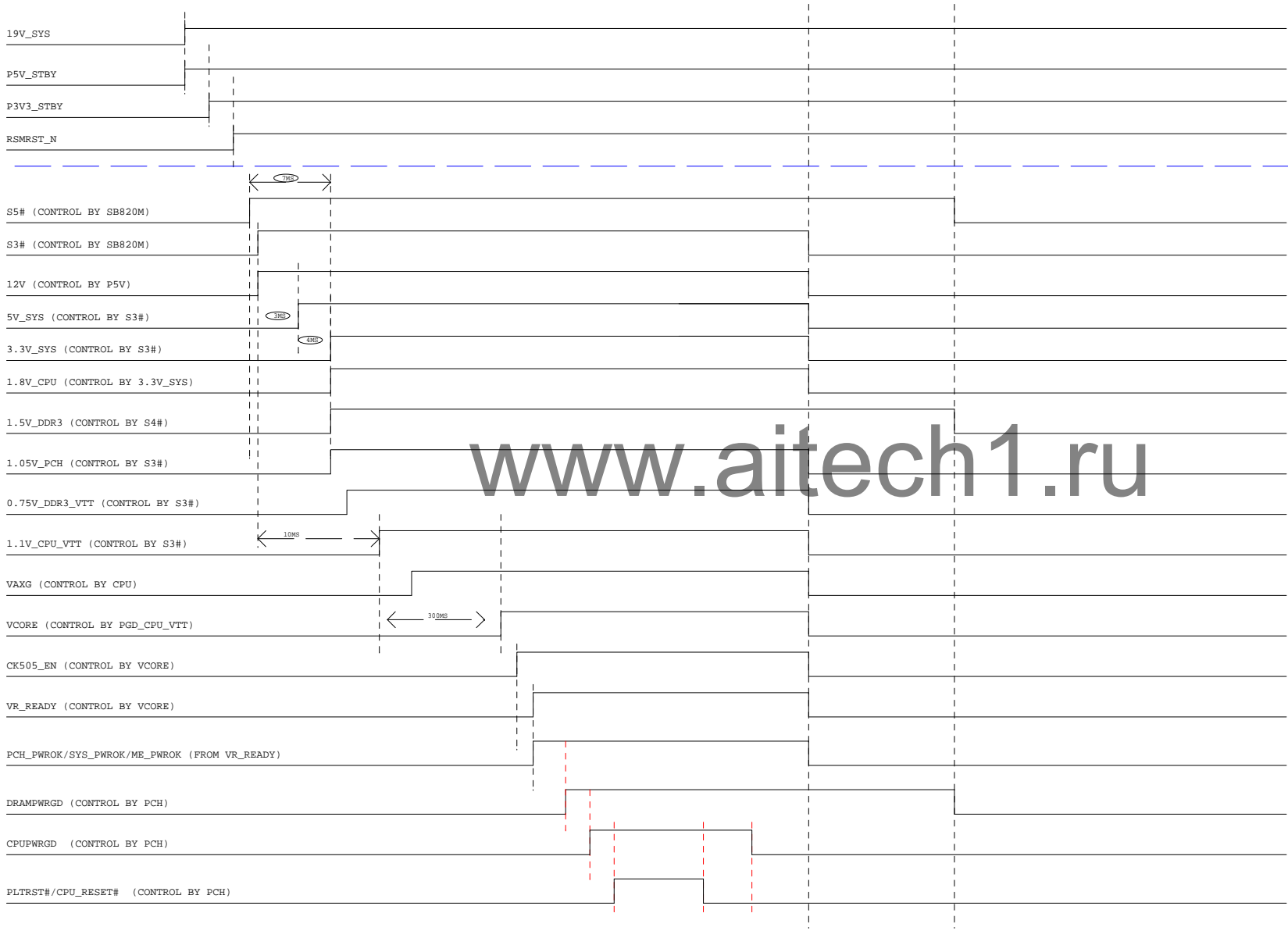


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# RESET SEQUENCE DIAGRAM

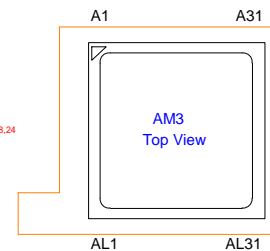


# Power on/down Sequency



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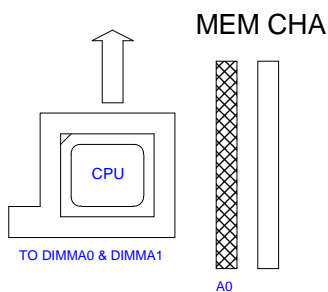
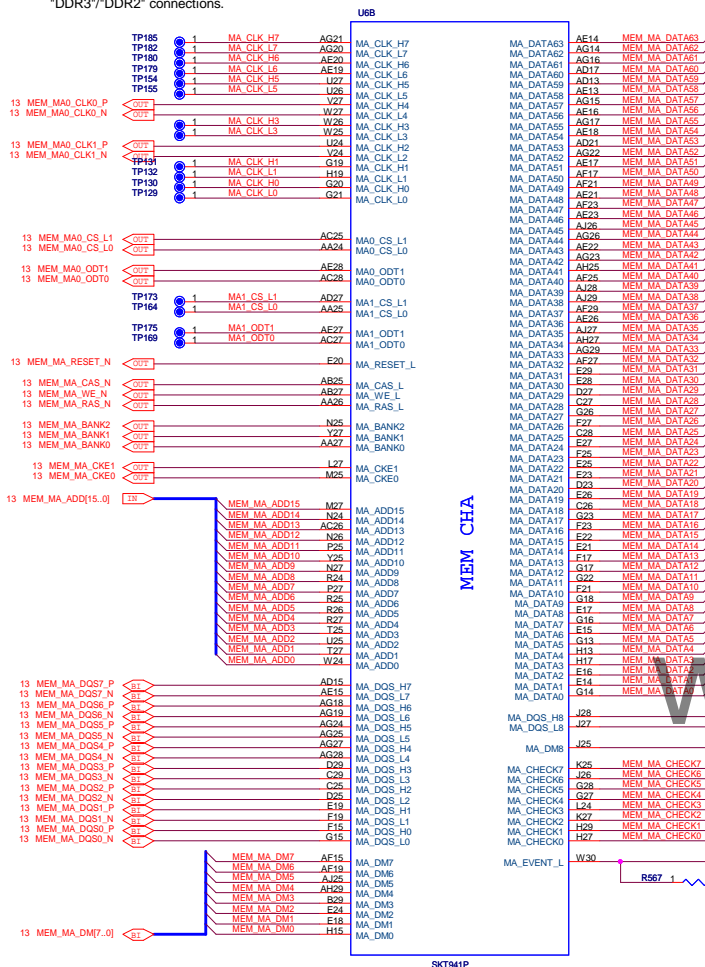
## HyperTransport



## CPU Memory

## DDR3 Memory Interface A

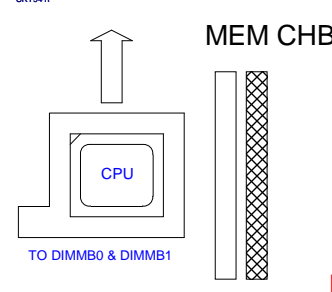
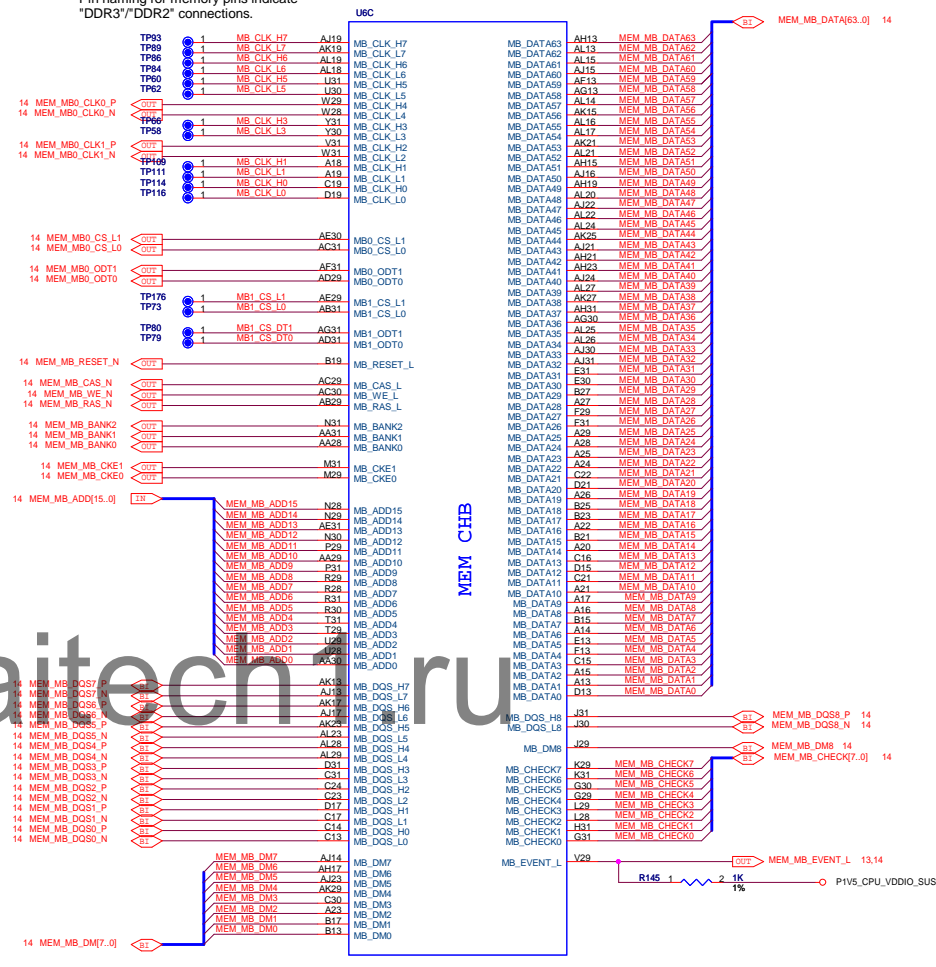
Pin naming for memory pins indicate "DDR3"/"DDR2" connections.



MEMORY CLOCK TRANSLATION			
DIMM	DDR3 Memory Signal		CPU Signal
DIMM A0	MEM_MA0_CLK1		MA_CLK2
	MEM_MA0_CLK0		MA_CLK4
DIMM B0	MEM_MB0_CLK1		MB_CLK2
	MEM_MB0_CLK0		MB_CLK4

## DDR3 Memory Interface B

Pin naming for memory pins indicate "DDR3"/"DDR2" connections.

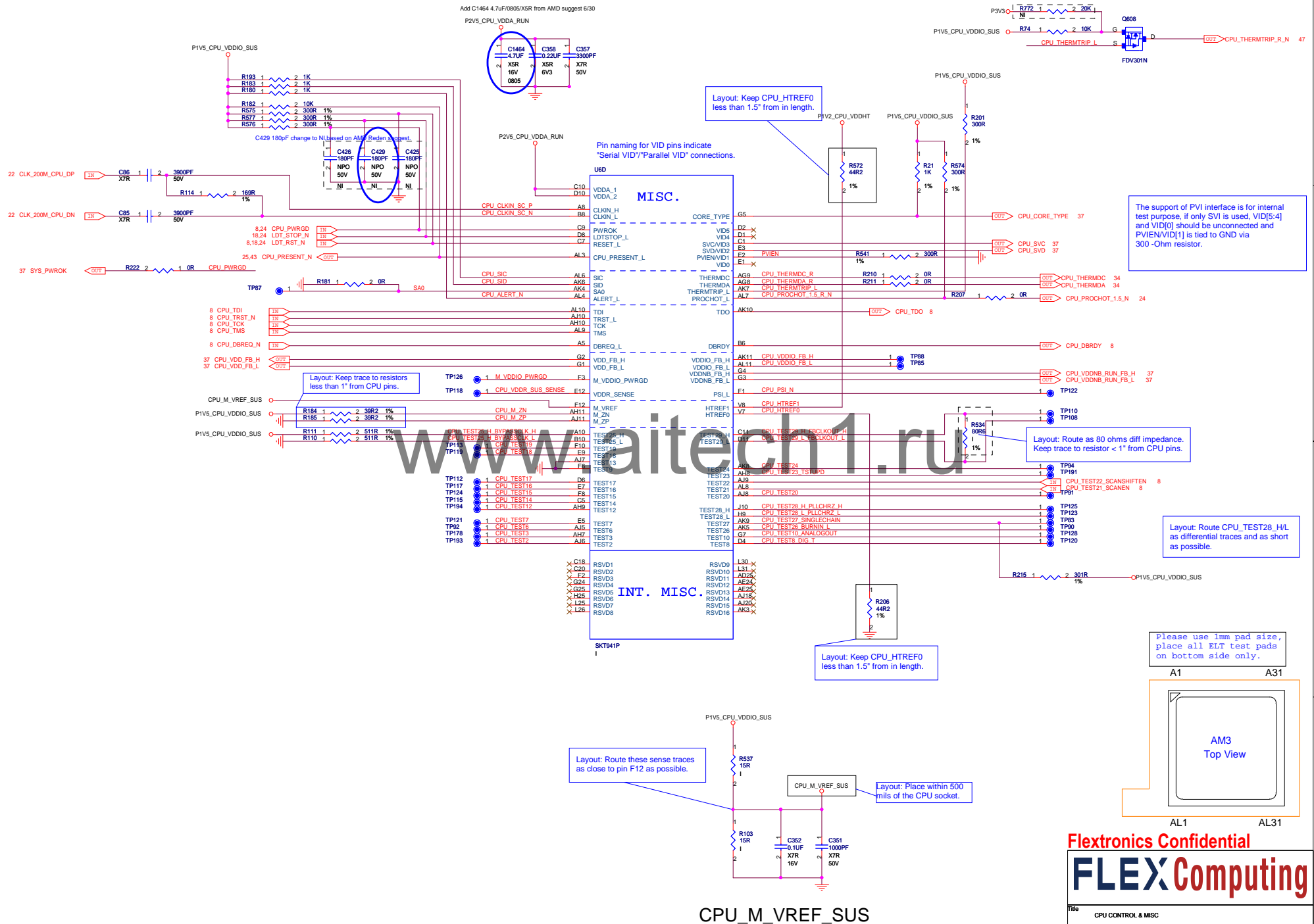


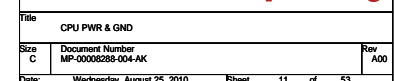
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CPU MEMORY			
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## CPU Control and Miscellaneous



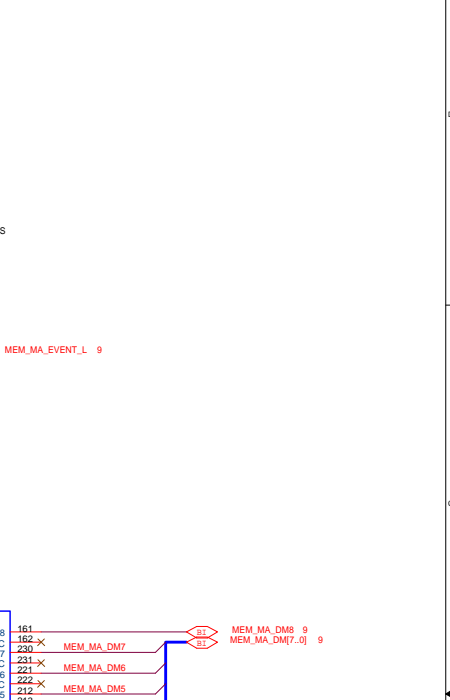
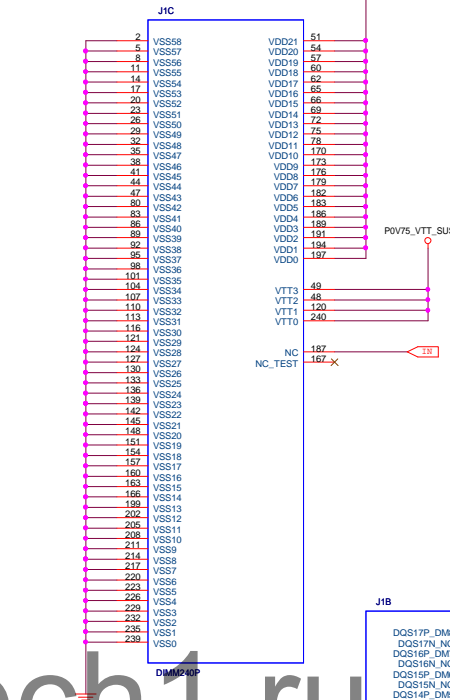
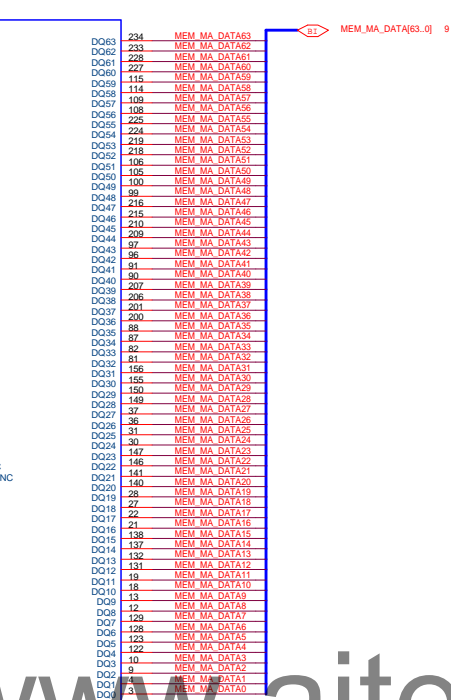
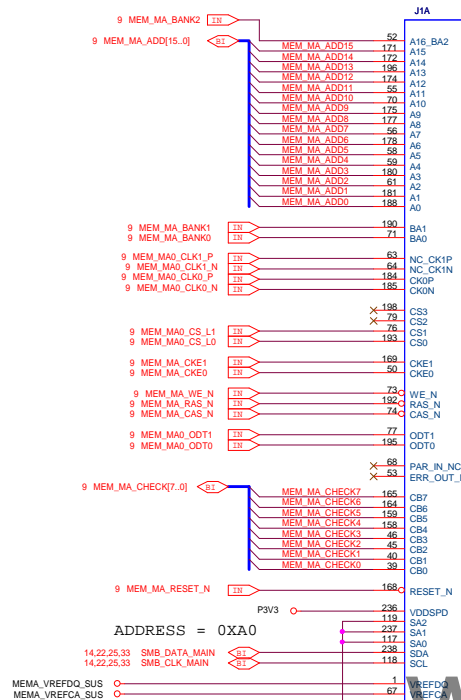


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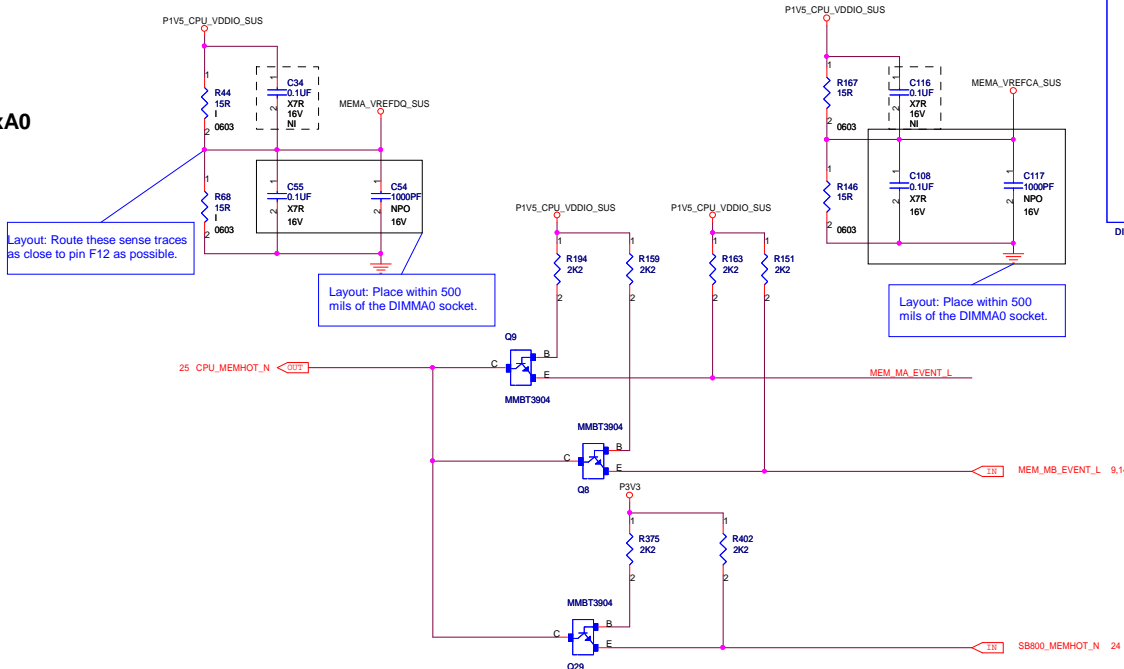
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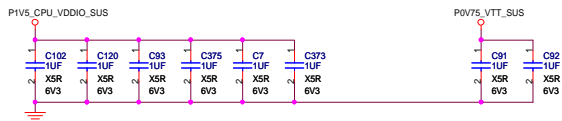
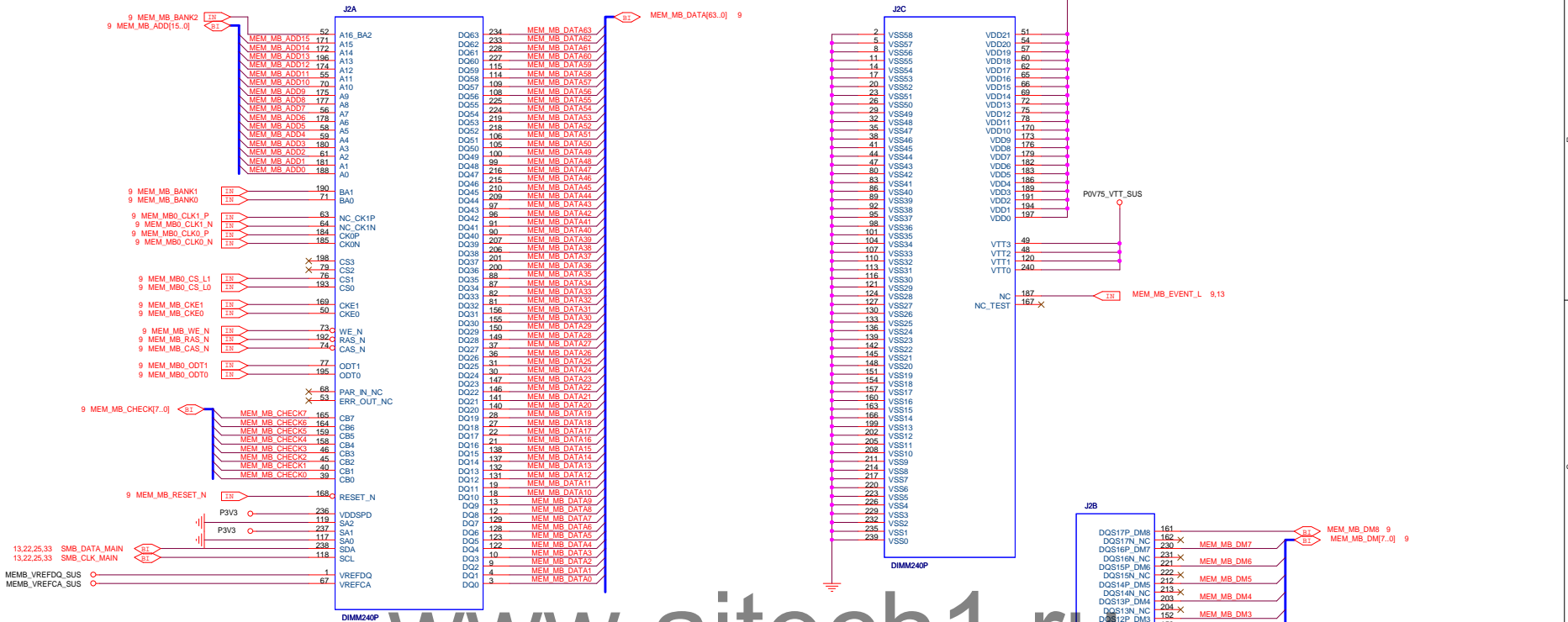


**DIMM - SPD SMBUS Address = 0xA0**

**SMBus Addressing**

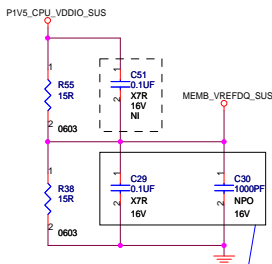
SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2



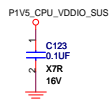


DE-COUPLING CAP FOR DIMMS

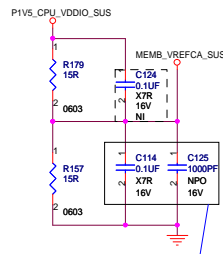
MEMB\_VREFDQ\_SUS



Layout: Place within 500 mils of the DIMMB0 socket.



MEMB\_VREFCA\_SUS



Layout: Place within 500 mils of the DIMMB0 socket.

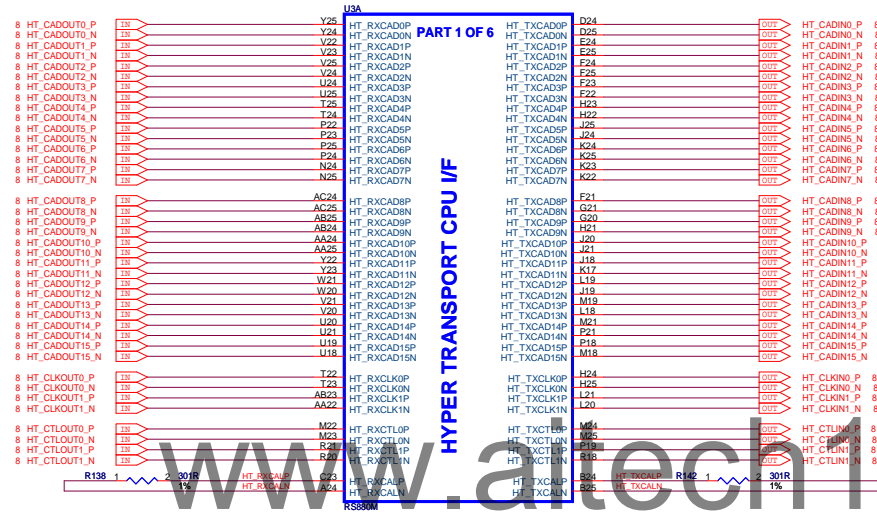
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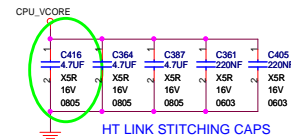
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\* RX780/RS780/RS880 difference table (HT LINK)

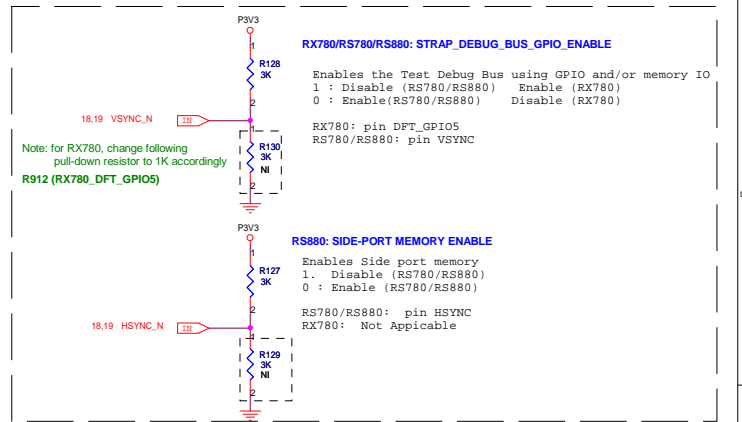
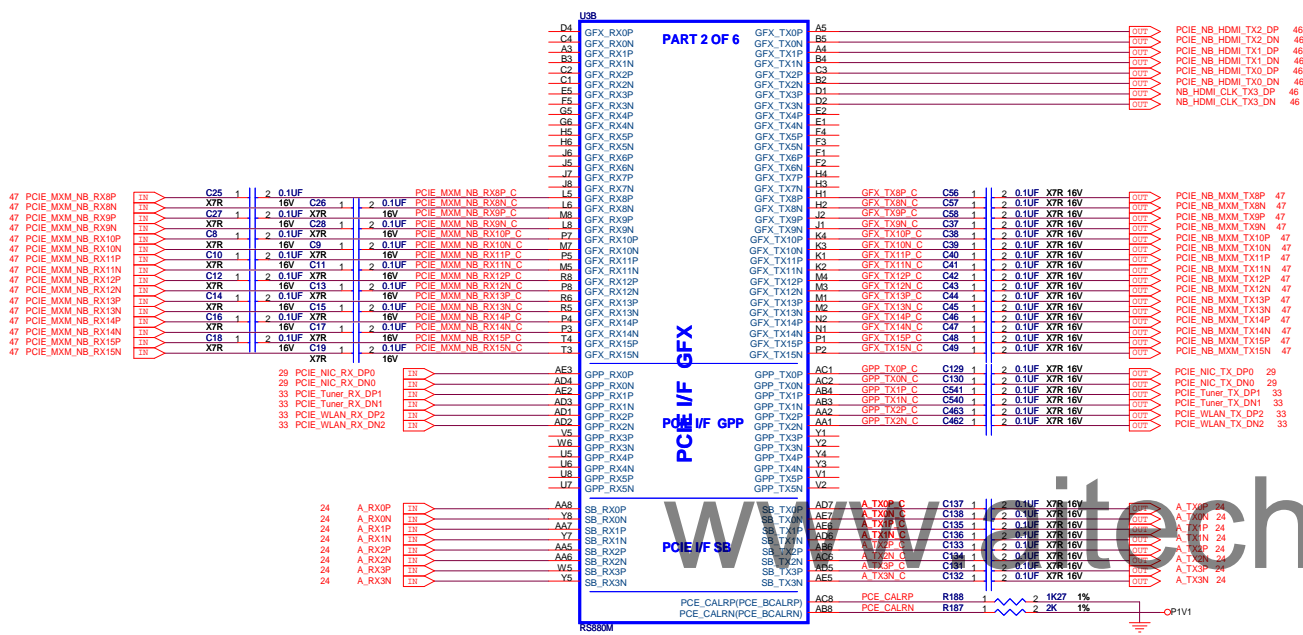
SIGNALS		RX780	RS780/880
HT_RXCALP	R69	1.21K	301R
HT_RXCALN			
HT_TXCALP	R70	1.21K	301R
HT_TXCALN			



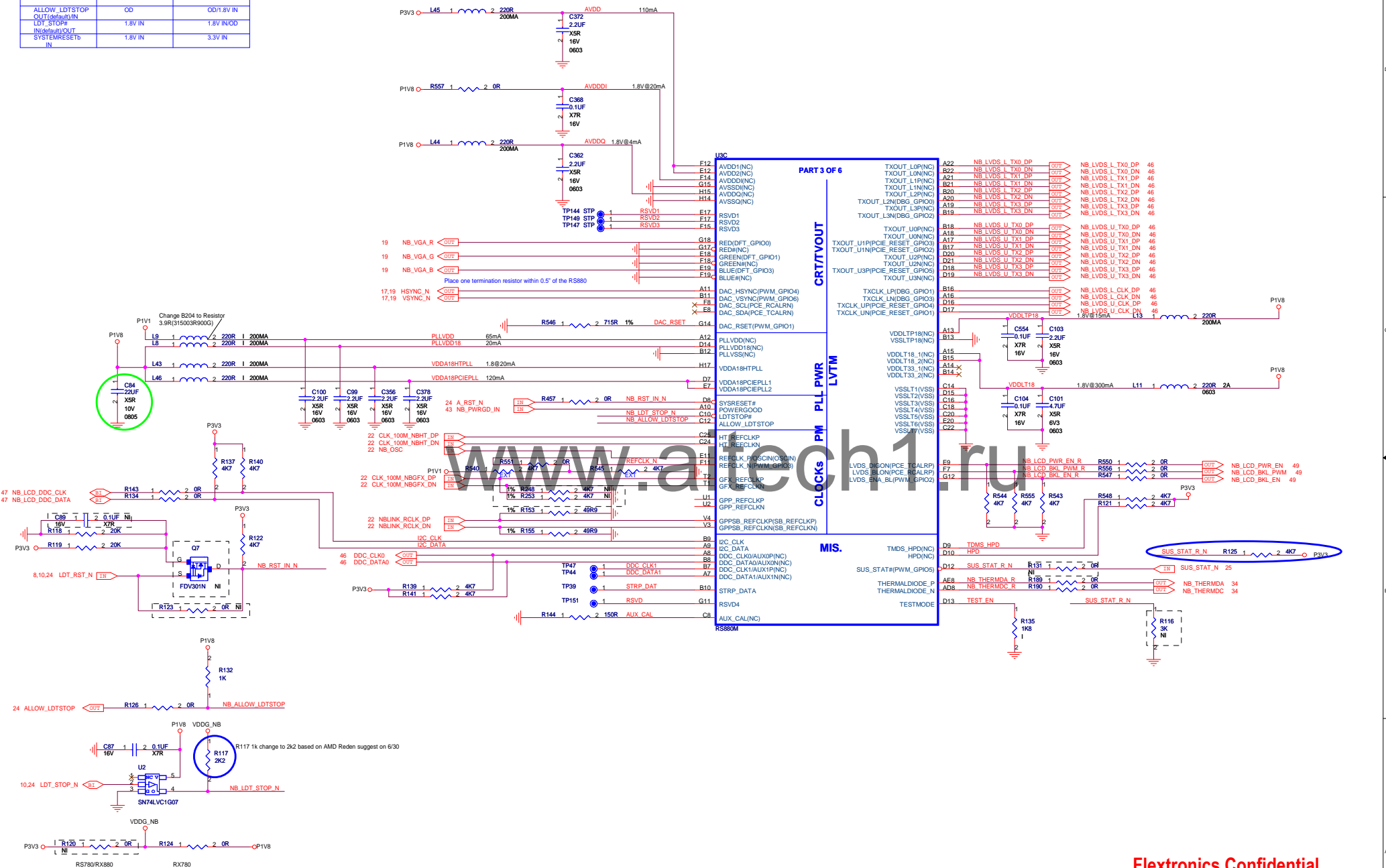
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Title			NB RS880M-HT LINK I/F	
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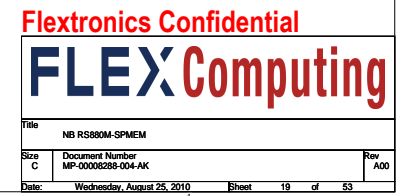
	RX760	RS760/RS680
NB_PWRGD IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)IN	OD	OD/1.8V IN
LDT_STOP# IN(default)OUT	1.8V IN	1.8V IN/OD
SYSTEMRESETb IN	1.8V IN	3.3V IN



	RX780	RS780/RS880
TRST(TP252)	TEST_EN	TEST_EN
TMS	PCIE_RST3(TP222)	DDC_DATA0(TP236)
TD(TP253)	I2C_DATA	I2C_DATA
TCK(TP254)	I2C_CLK	I2C_CLK
TDO	PWM_GPIO6(TP219)	TMDS_HPD(TP221)

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NB RS880M-HDMI/VGA			
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PIN NAME	RX780	RS70/RS80	PIN NAME	RX780	RS70/RS80
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTFX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDI18	+1.8V	+1.8V	PLVDD	NC	+1.1V
VDDI18_MEM	NC	+1.8V	PLVDDI18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.5V(DDR3)	VDDLTP18	NC	+1.8V
VDD33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC



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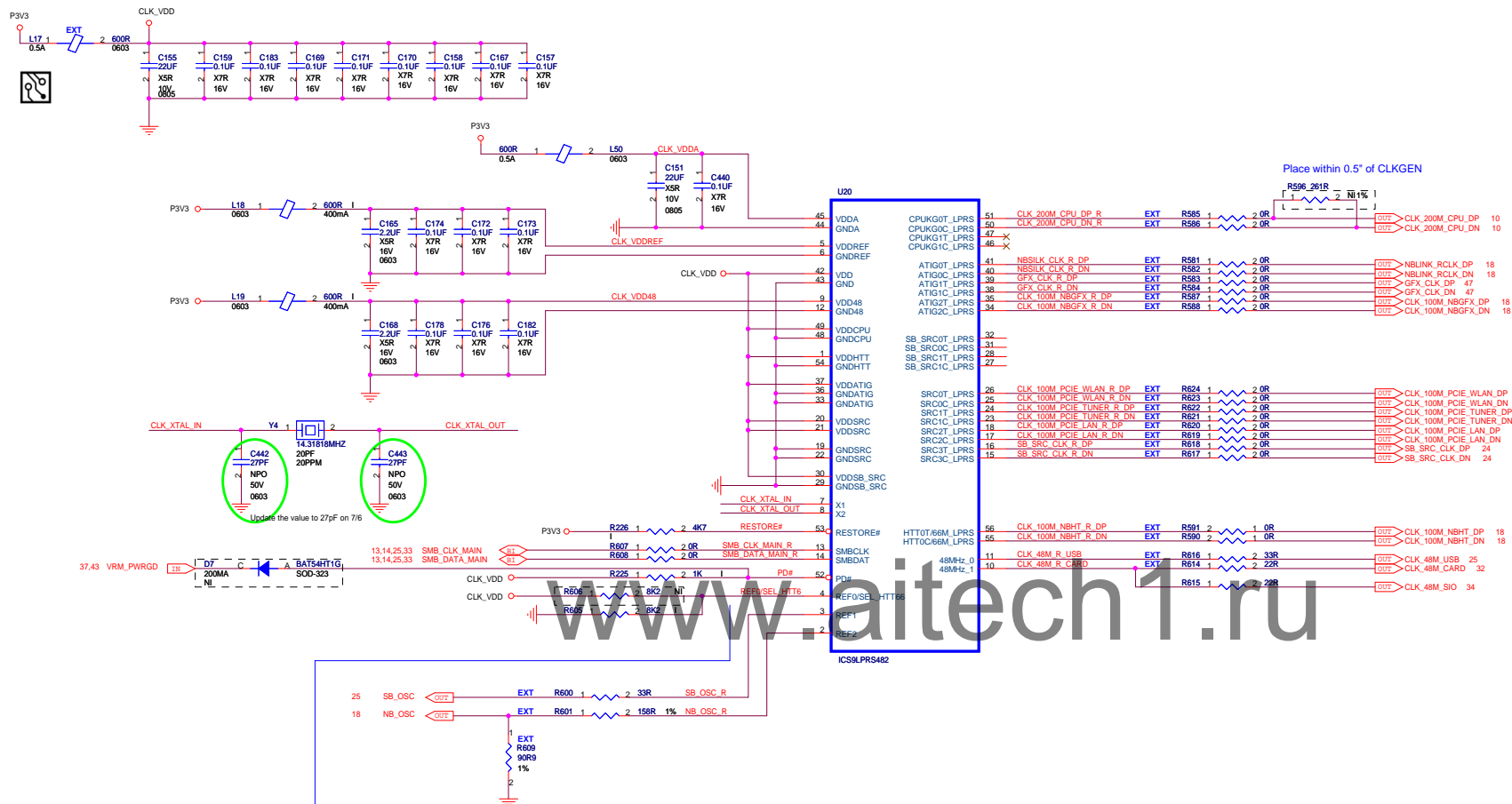
Title			NB RS880M POWER		
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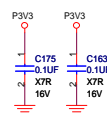
REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

Default

NB CLOCK INPUT TABLE

NB CLOCKS	RS880M
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	14M SE (1.1V)
GFX_REFCLK	100M DIFF (IN/OUT)
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

\* RS780M can be used as clock buffer to output two PCIe reference clocks. By default, chip will configured as input mode, BIOS can program it to output mode.



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File		
CLOCK GENERATOR		
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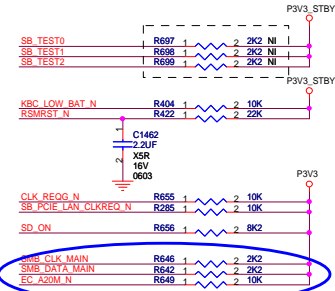
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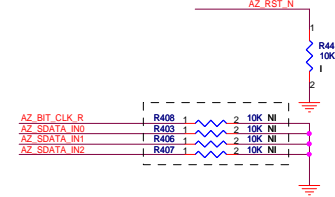
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SB820M SB\_TEST0,SB\_TEST1,SB\_TEST2 has internal 10K PD

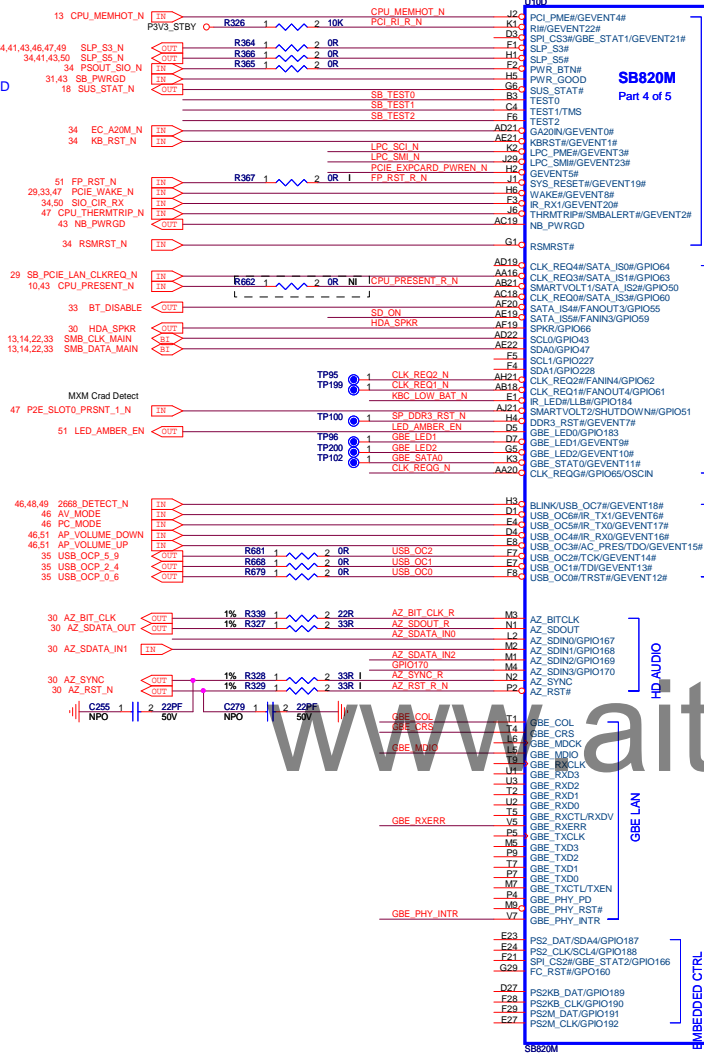
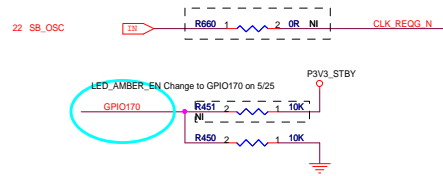
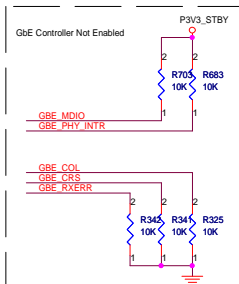
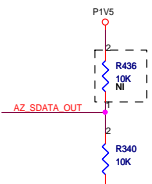


EC\_A20M\_N connect to P3V3 on 7/1

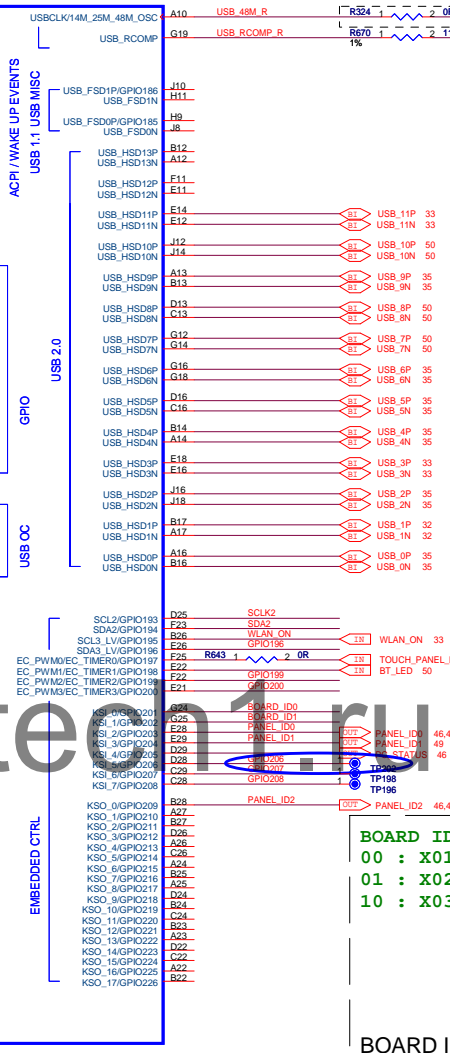


### REQUIRED STRAPS

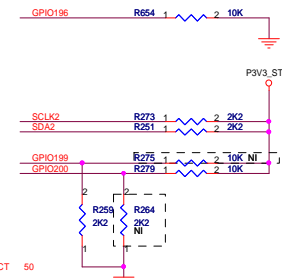
AZ_SDOUT	
PULL HIGH	LOW POWER MODE
PULL LOW	PERFORMANCE MODE DEFAULT



BOARD CONFIG					
NB/SB	EXT_CLK	GIGABIT	DVI	HDMI	SPMEM
RS880/SB810	YES	57780	NO	YES	SAMSUNG

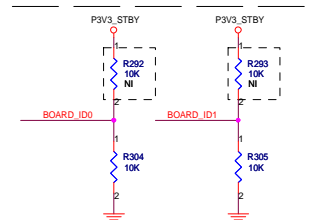


USB Assign	Function
Port 0,6	Side I/O
Port2,4,5,9	Rear I/O
Port 1	Card Reader Controller
Port 3	WLAN
Port 7	Touch
Port 8	Camera
Port 10	BlueTooth
Port 11	TV Tuner



GPIO199	GPIO200	ROM TYPE
H	H	Reserved
L	H	SPI ROM
H	L	LPC ROM
L	L	FWH ROM

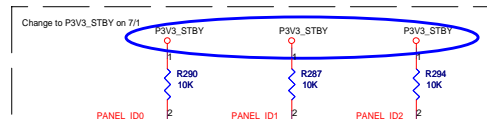
**DEFAULT**



BOARD ID1/ID0

```
00 : x01
01 : x02
10 : x03
```

BOARD ID jumper



PANEL ID jumper

```
BOARD Panel ID2 /ID1/ ID0
100 : SUMSANG 23"
101 : LG 23"
110 : SUMSANG 21.5"
111 : LG 21.5"
0** : for Extra Vendor
```

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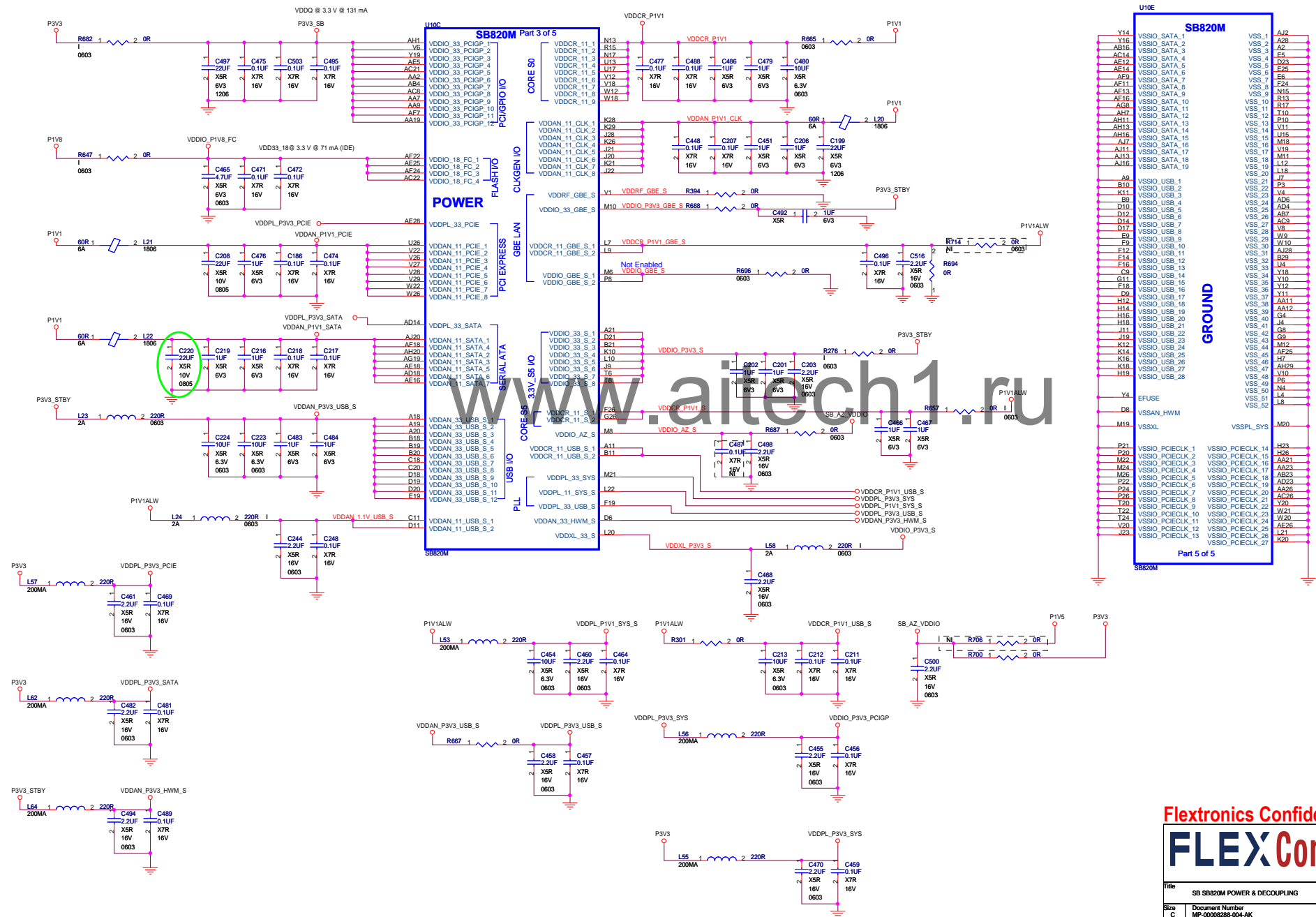
# FLEX Computing

Title			
SB SB820M GPIO/USB/AUDIO			
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PLACE ALL THE DECOUPLING CAPS ON  
THIS SHEET CLOSE TO SB AS POSSIBLE.



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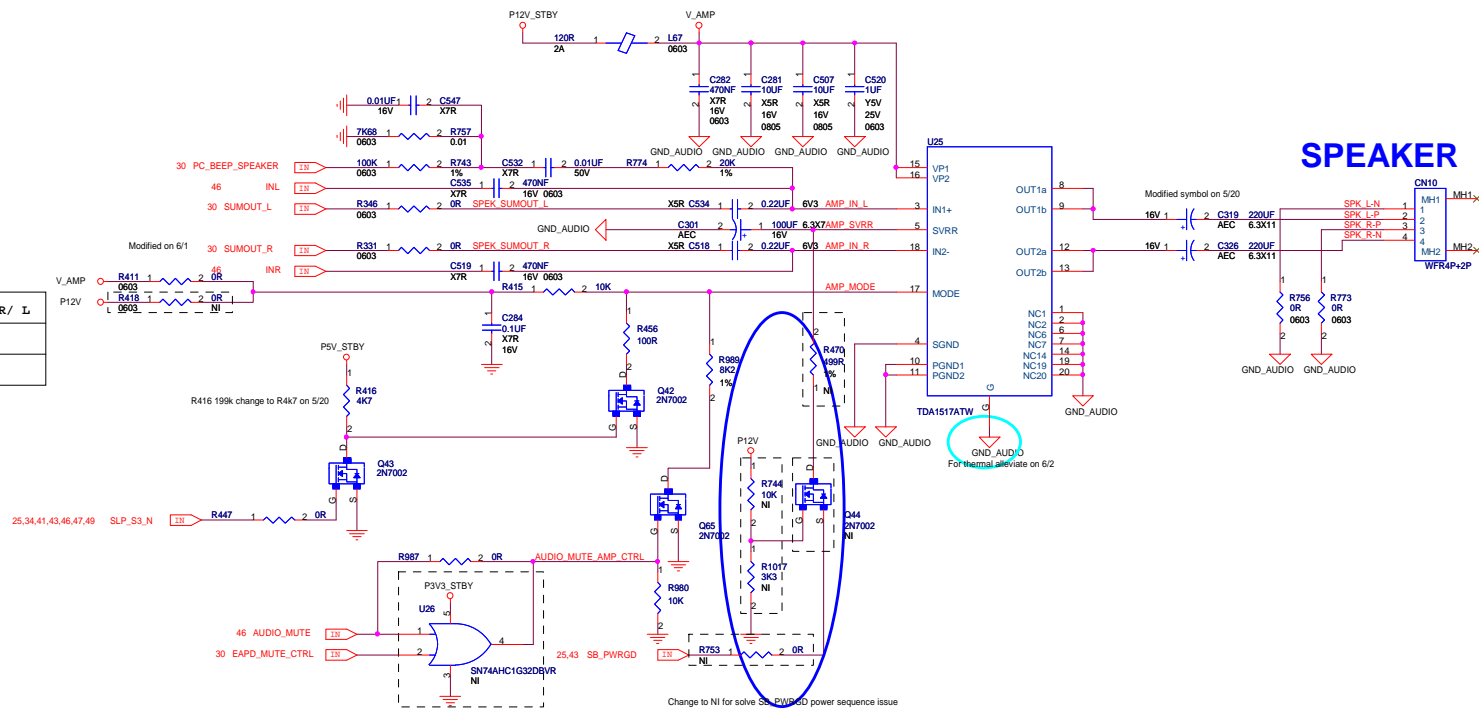
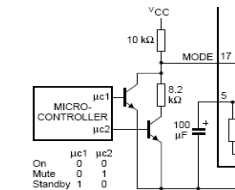
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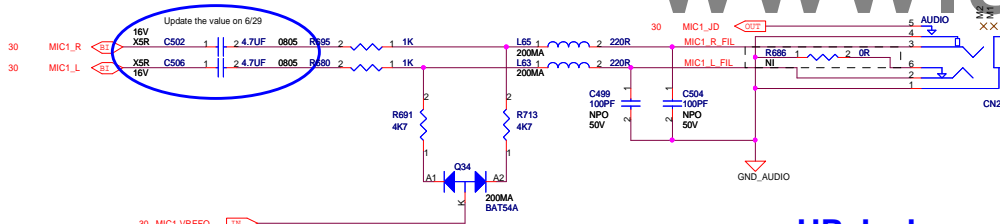




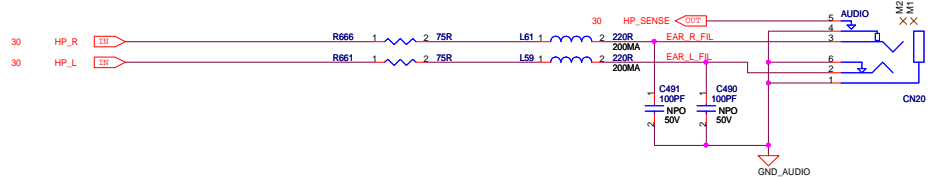
# Audio AMP / SPKR



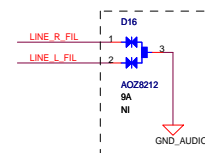
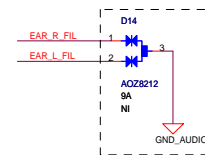
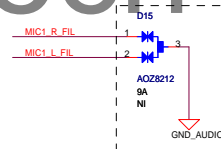
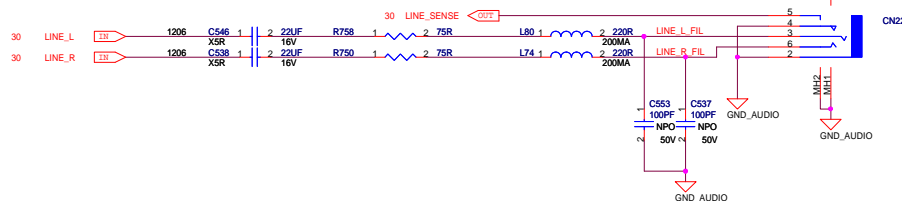
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## HP Jack



## Line-out JACK

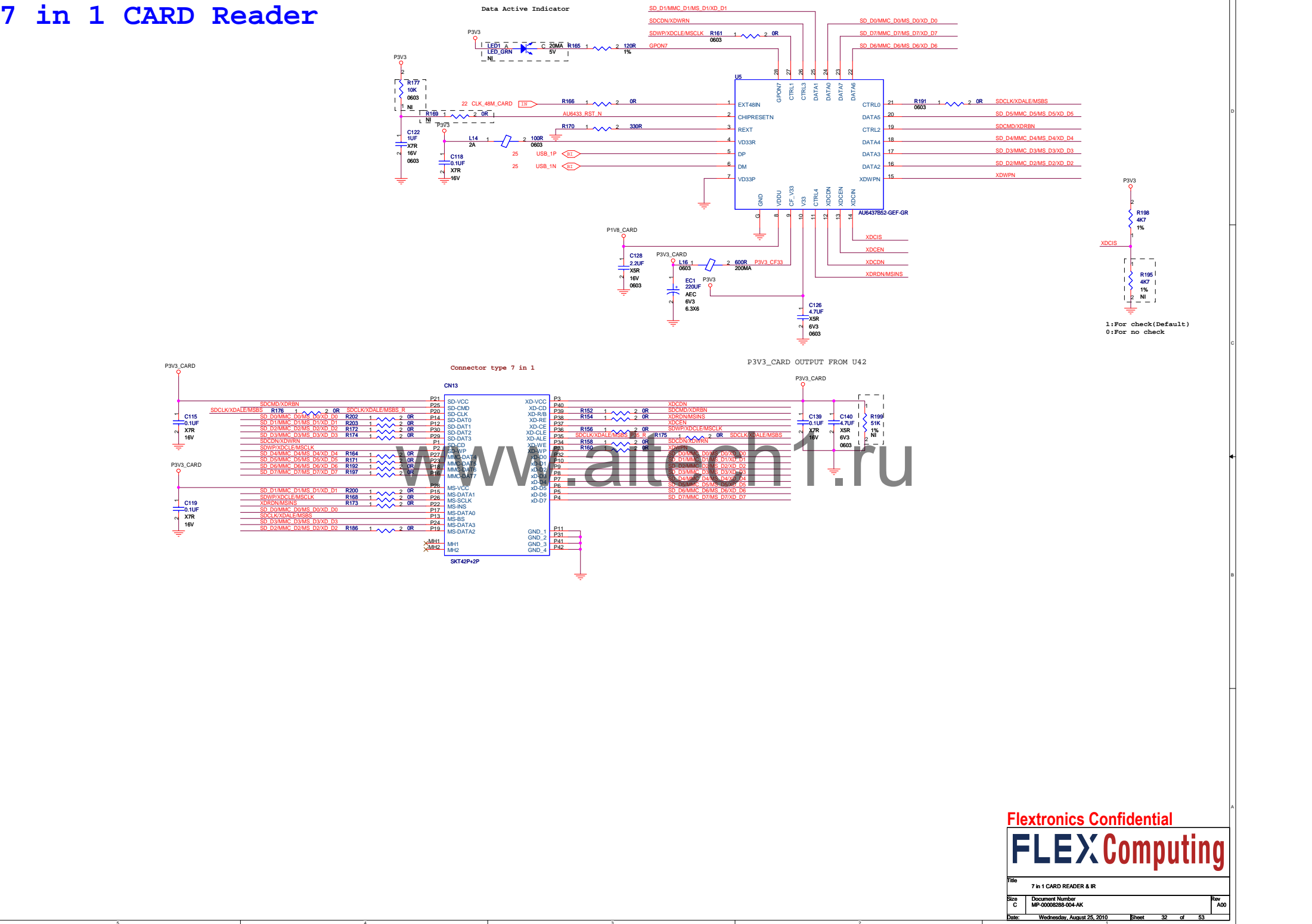


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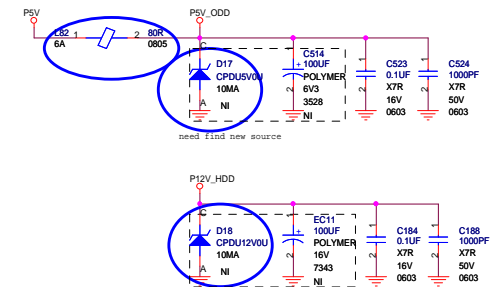
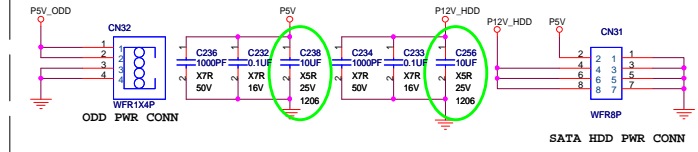
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Title			AMP & HP & SPOIF & L-Out
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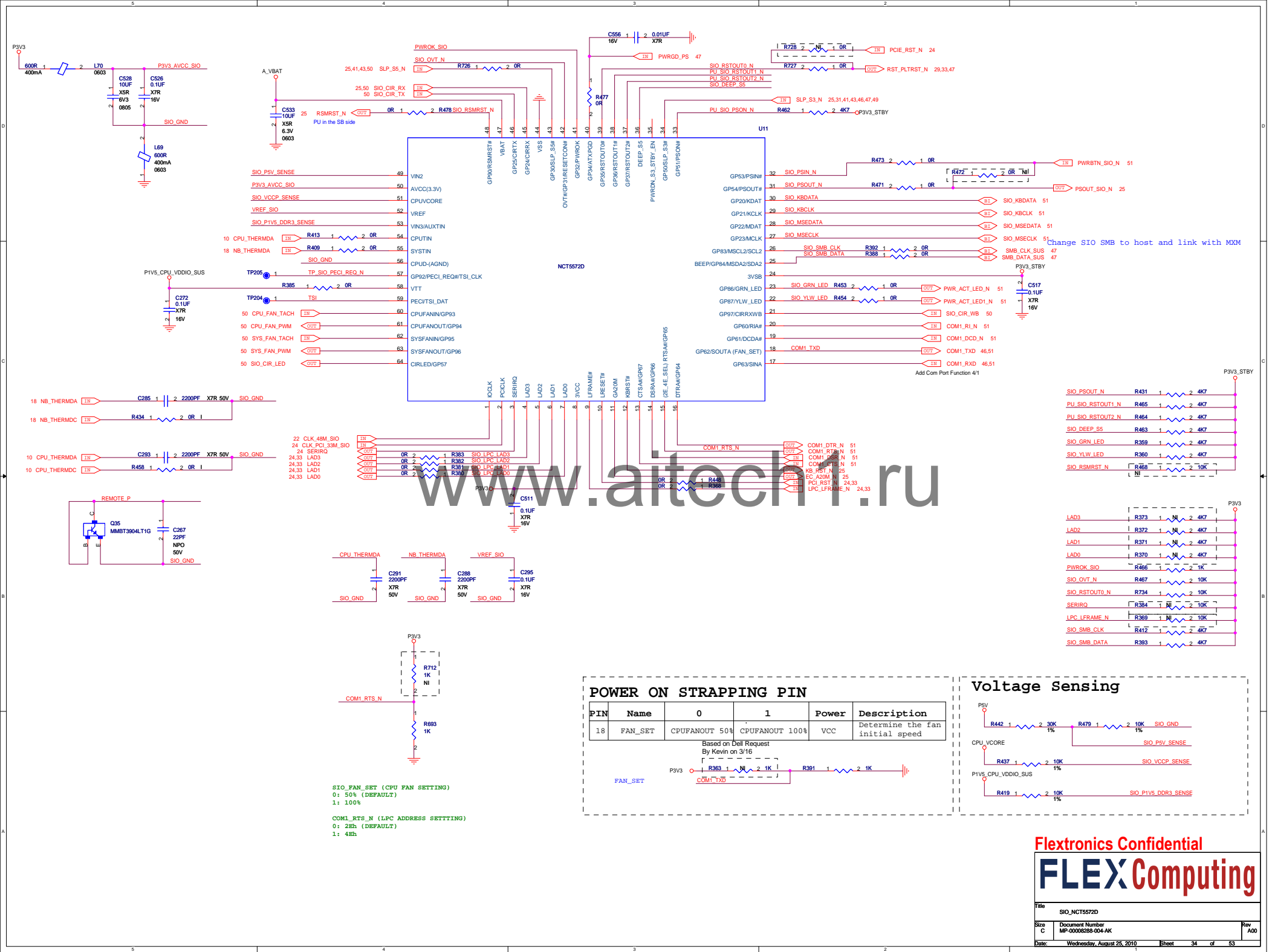
7 in 1 CARD Reader



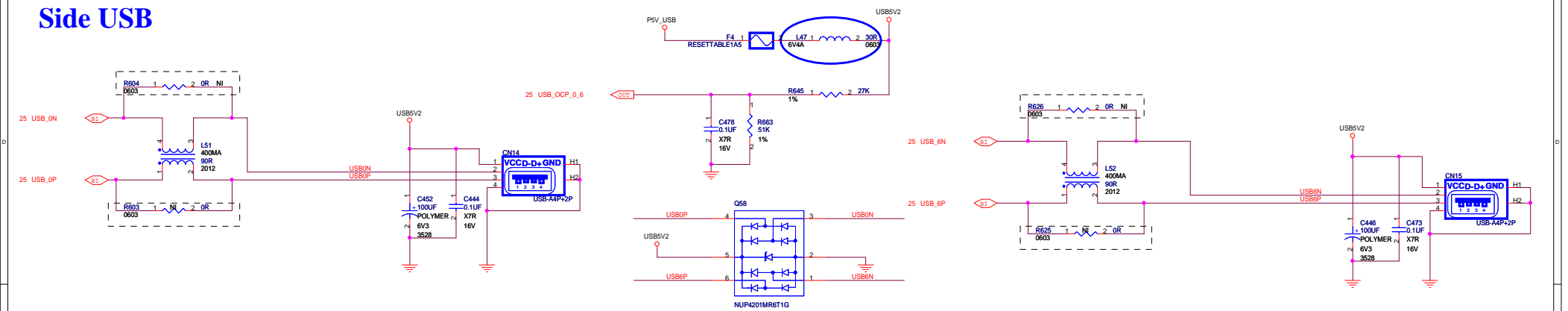
17	PCIE_Tuner_TX_DP1	1N	33
17	PCIE_Tuner_TX_DN1	1N	31
17	PCIE_Tuner_RX_DP1	OUT	25
17	PCIE_Tuner_RX_DN1	OUT	23
22	CLK_100M_PCIE_TUNER_DP	1N	13
22	CLK_100M_PCIE_TUNER_DN	1N	11
PCIE TUNER CLKREQ_N			7
R486 1 2 OR PCIE_WAKE_TV_N			1



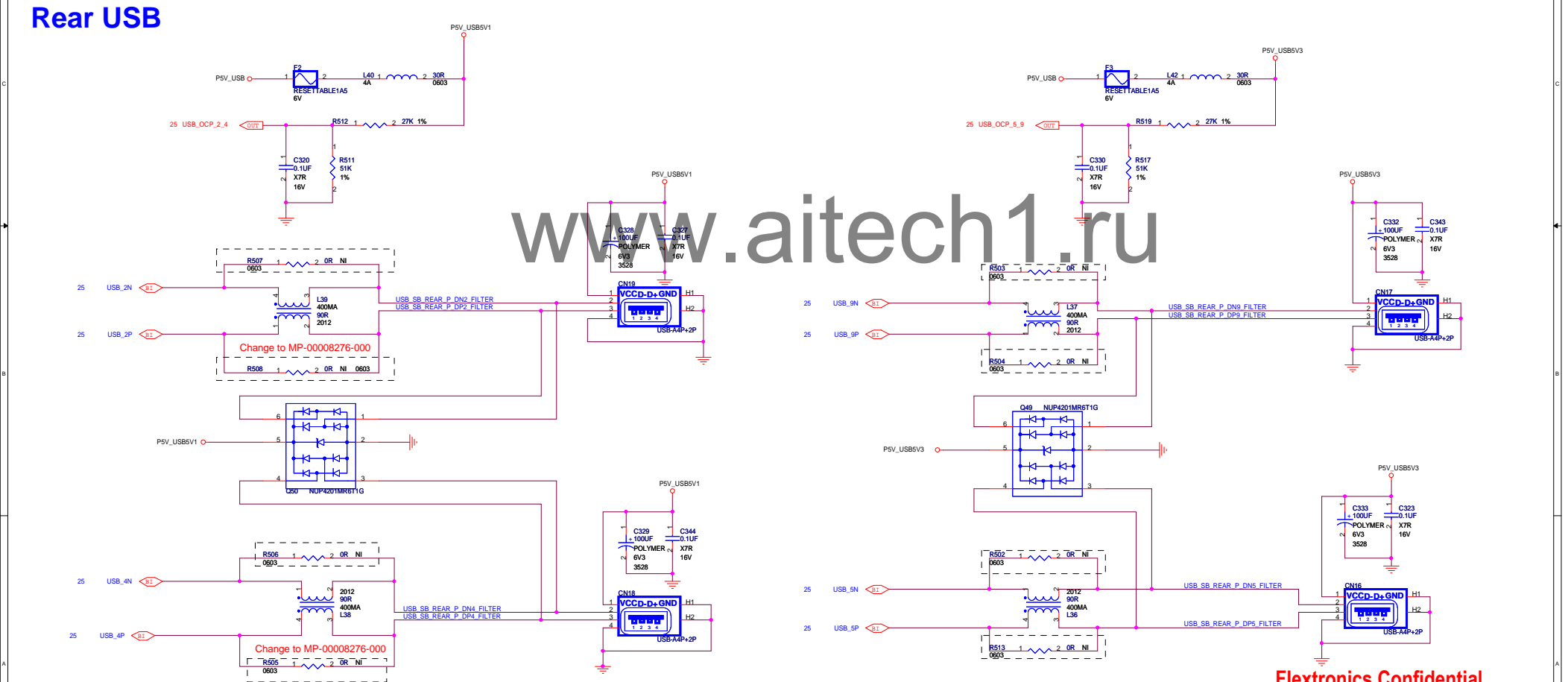
The logo features the word "Flextronics Confidential" in a red sans-serif font at the top. Below it is a large, stylized "FLEX" in blue with a red outline, followed by "Computing" in a red script font. At the bottom, a red horizontal bar contains the text "MiniPCIe WLAN&TVT&SATA" in white. Below this bar is a table with four columns: "Size C", "Document Number MP-00008288-004-AK", "Date Wednesday, August 25, 2010", and "Rev A00". The last two cells of the table are merged.



## Side USB



## Rear USB



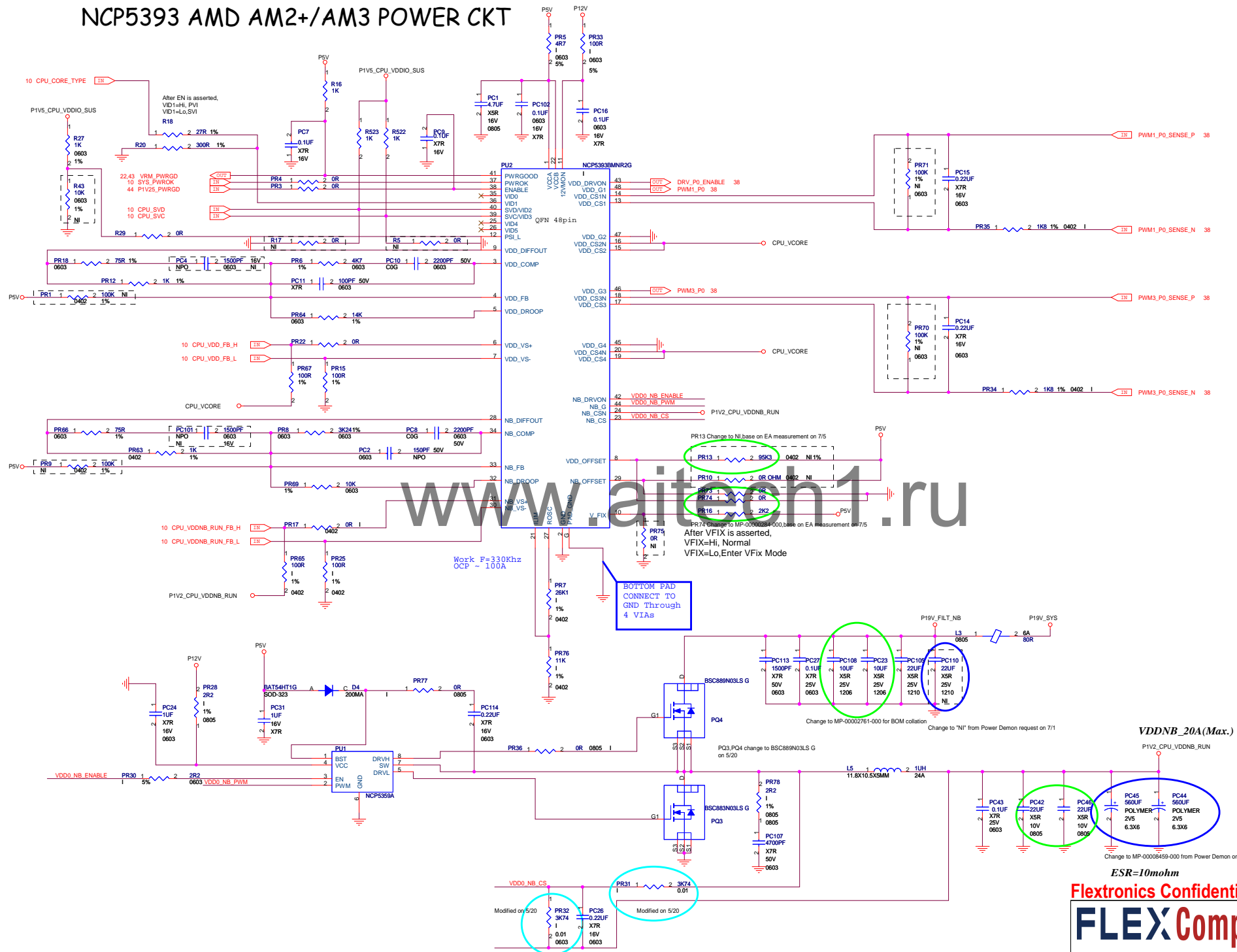
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# NCP5393 AMD AM2+/AM3 POWER CKT



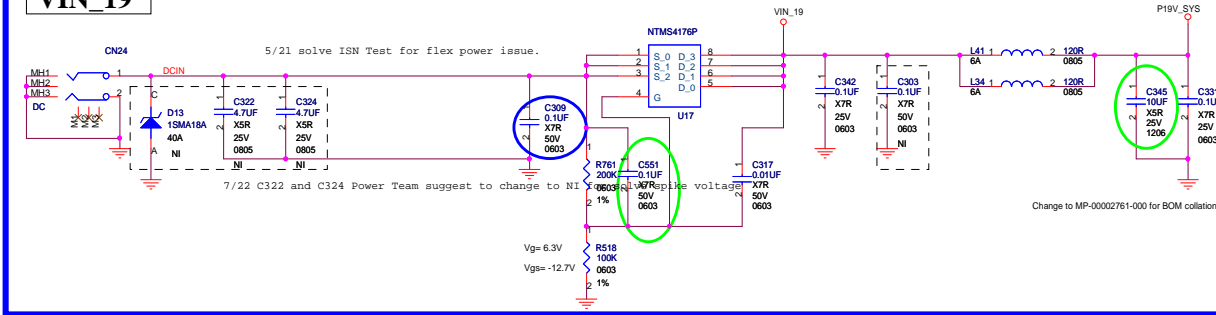
CLOSE PWM

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CPU Core PWM			
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# VIN\_19



Note:Delete L59,L60 and DCGND and change J12 ground to GND.

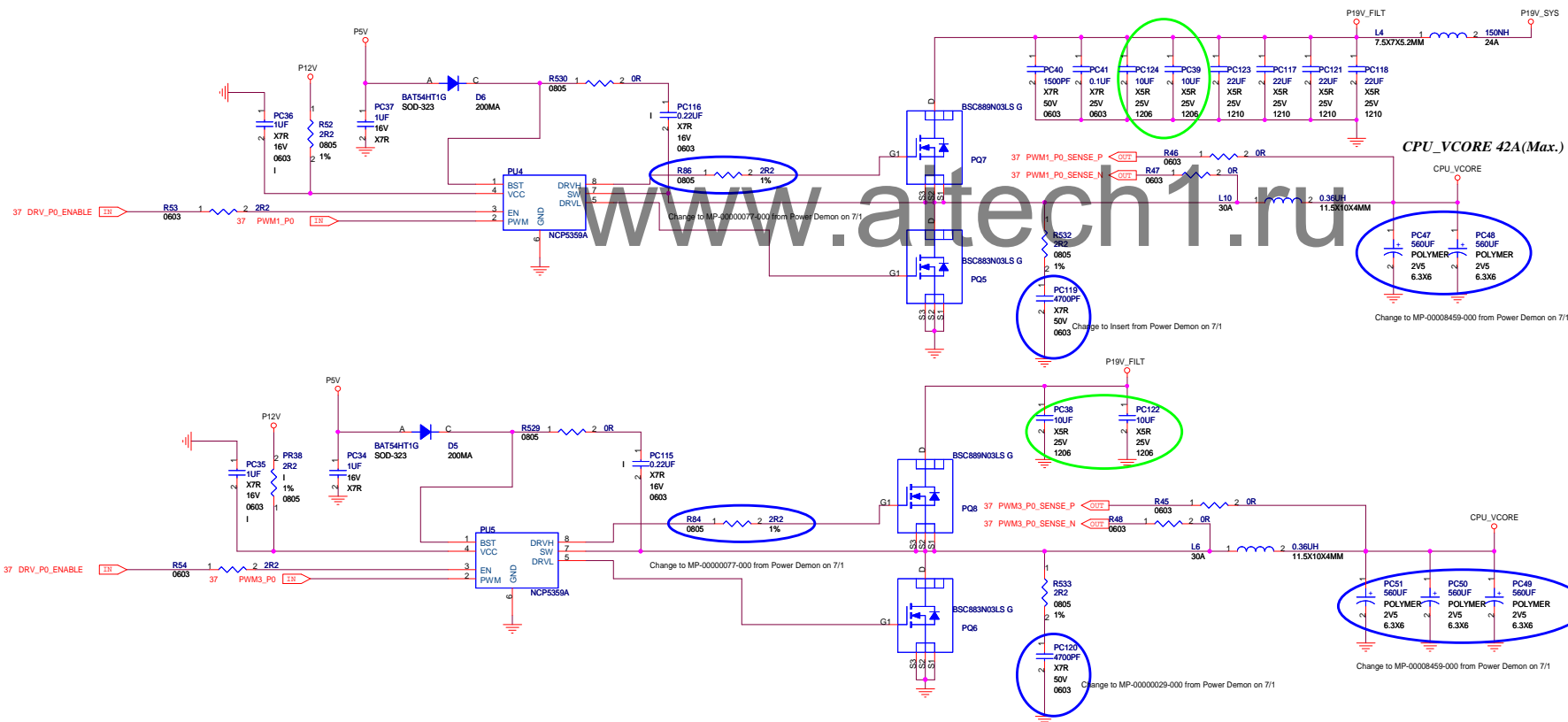
2009.0811

George Li

Note:Delete L59,L60 and DCGND and change J12 ground to GND.

2009.0811

George Li

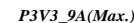


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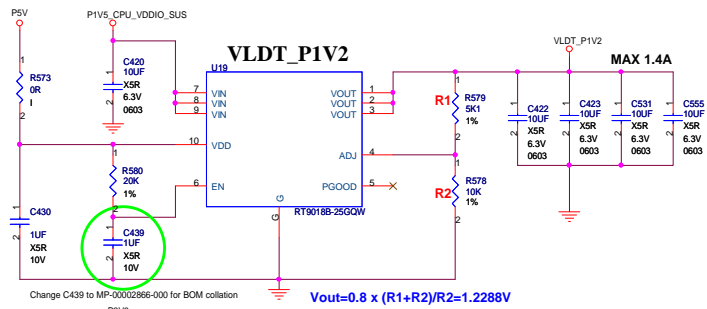
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VIN&VCC&VCC_NB		
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*P5V\_15A(Max.)*

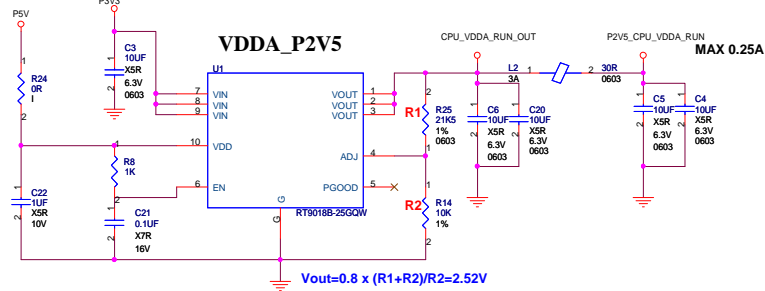
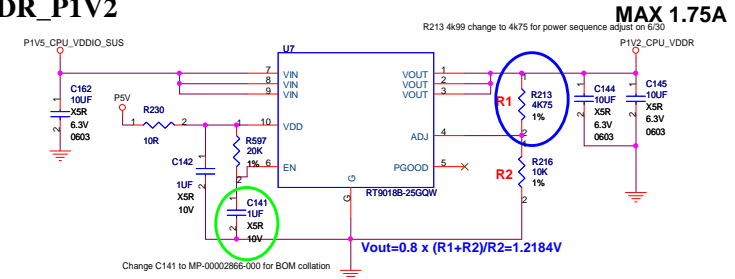


***ESR=25mohm***

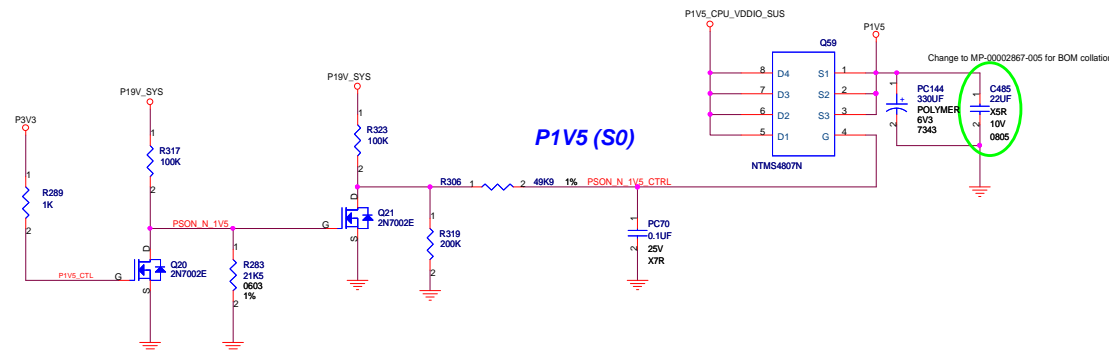
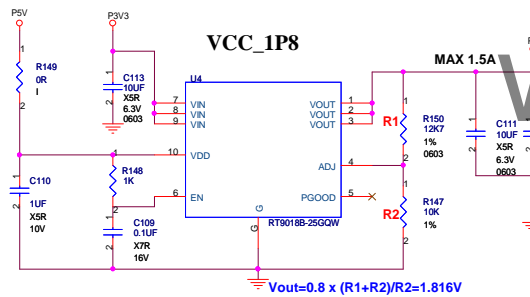
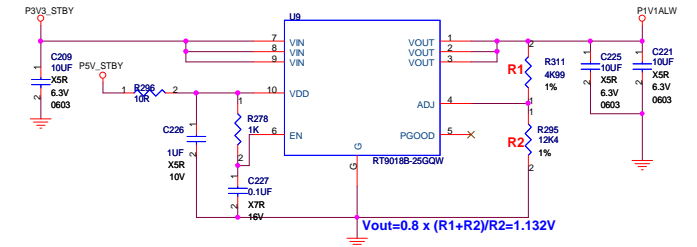
Change to MP-00009816-000 from Power Demon on 7/1



## VDD\_DDR\_P1V2



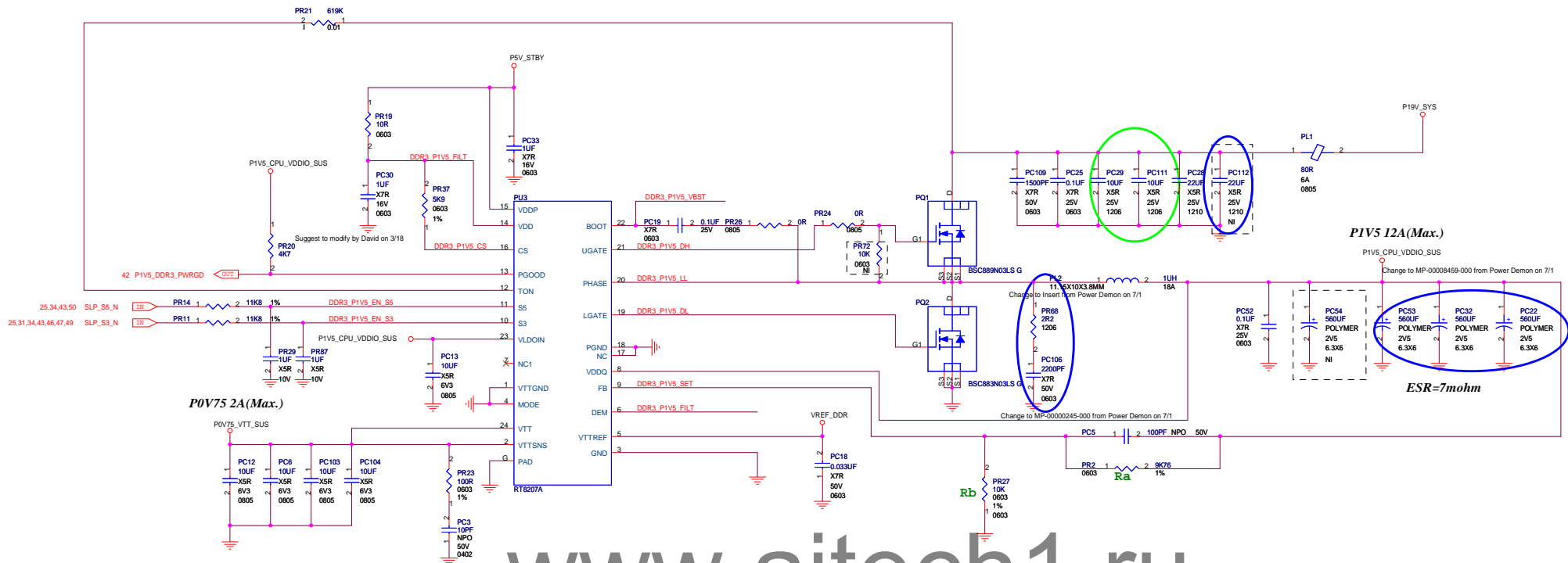
## P1V1\_STBY



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Title			P1V2 / P1V8 / P2V5 / P1V5
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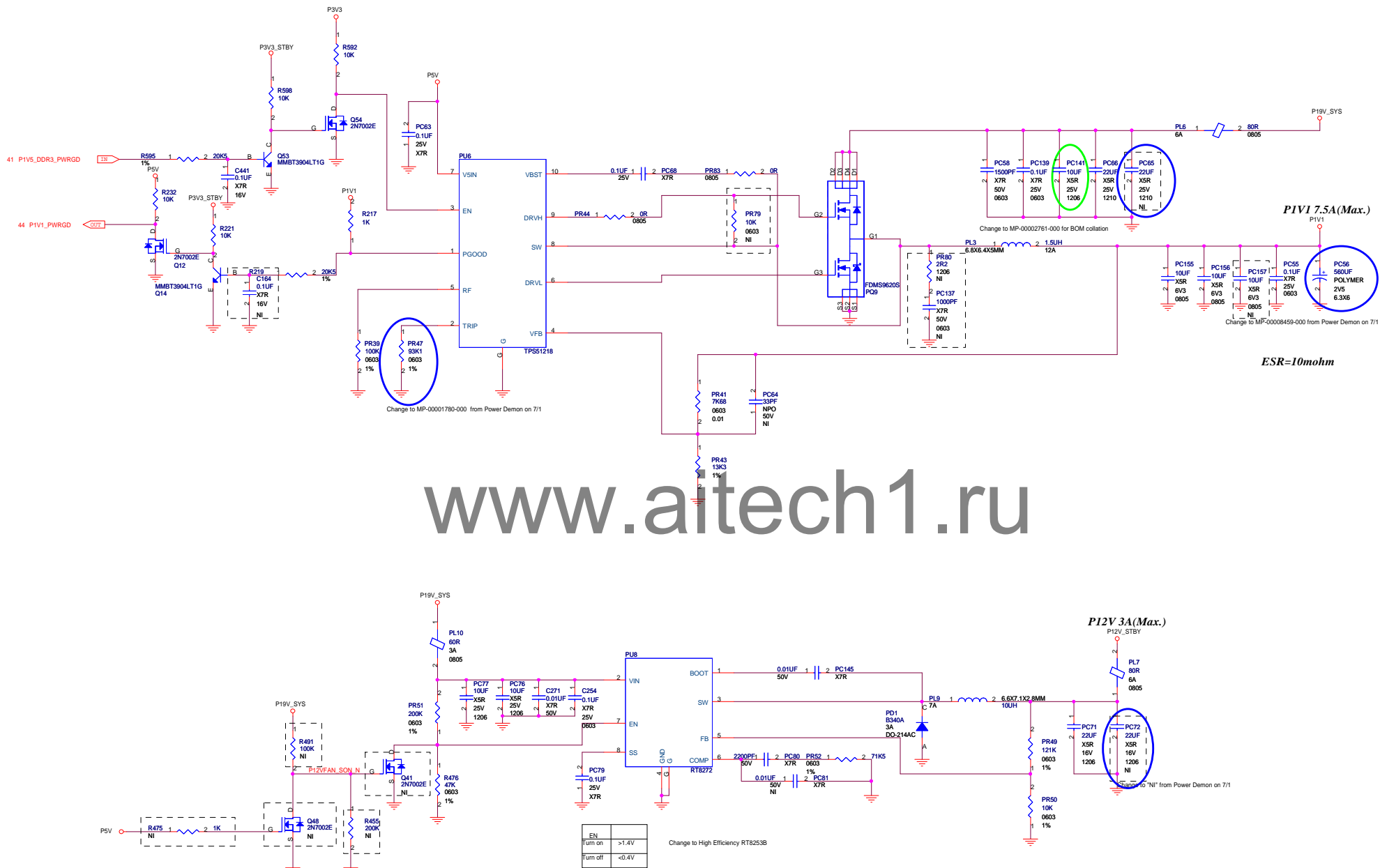
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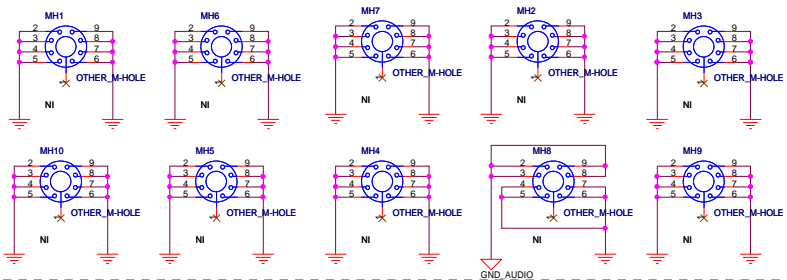
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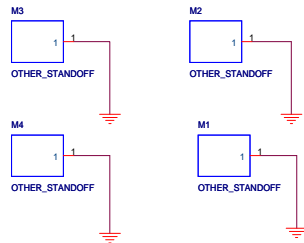




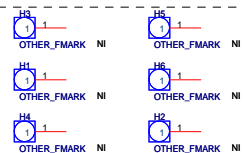
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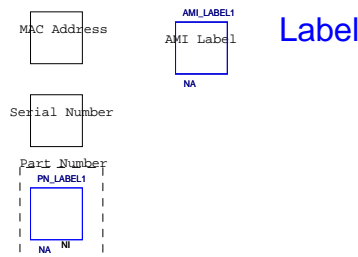
## FOR CPU HINTSINK



## FOR FIDUCIAL MARK



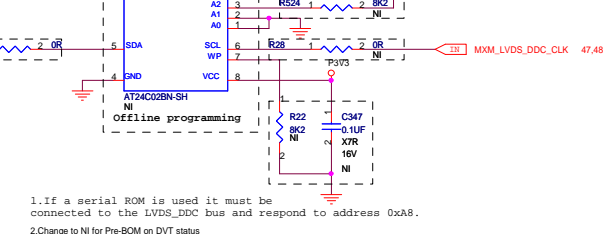
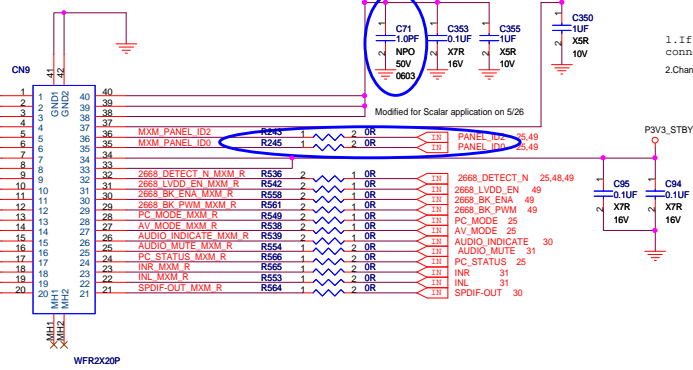
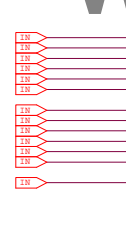
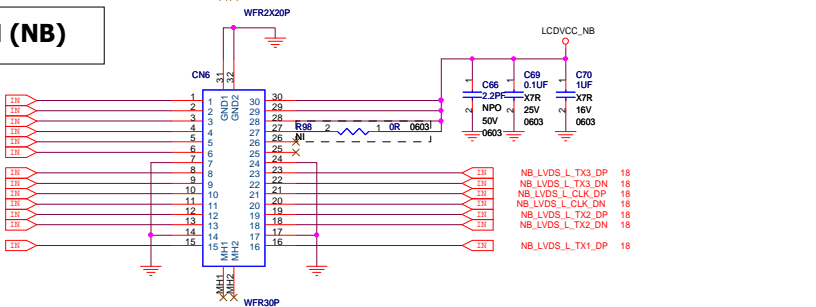
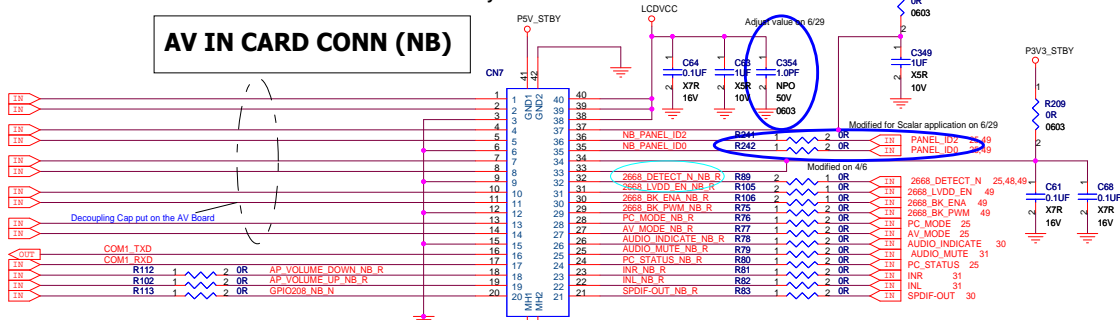
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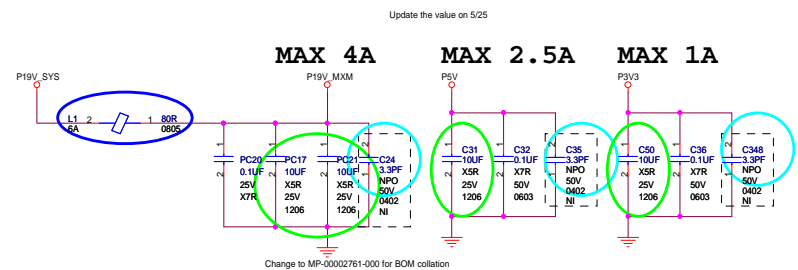
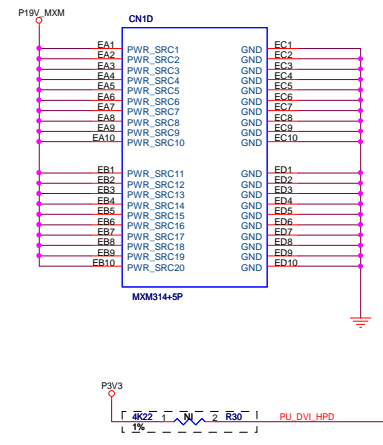
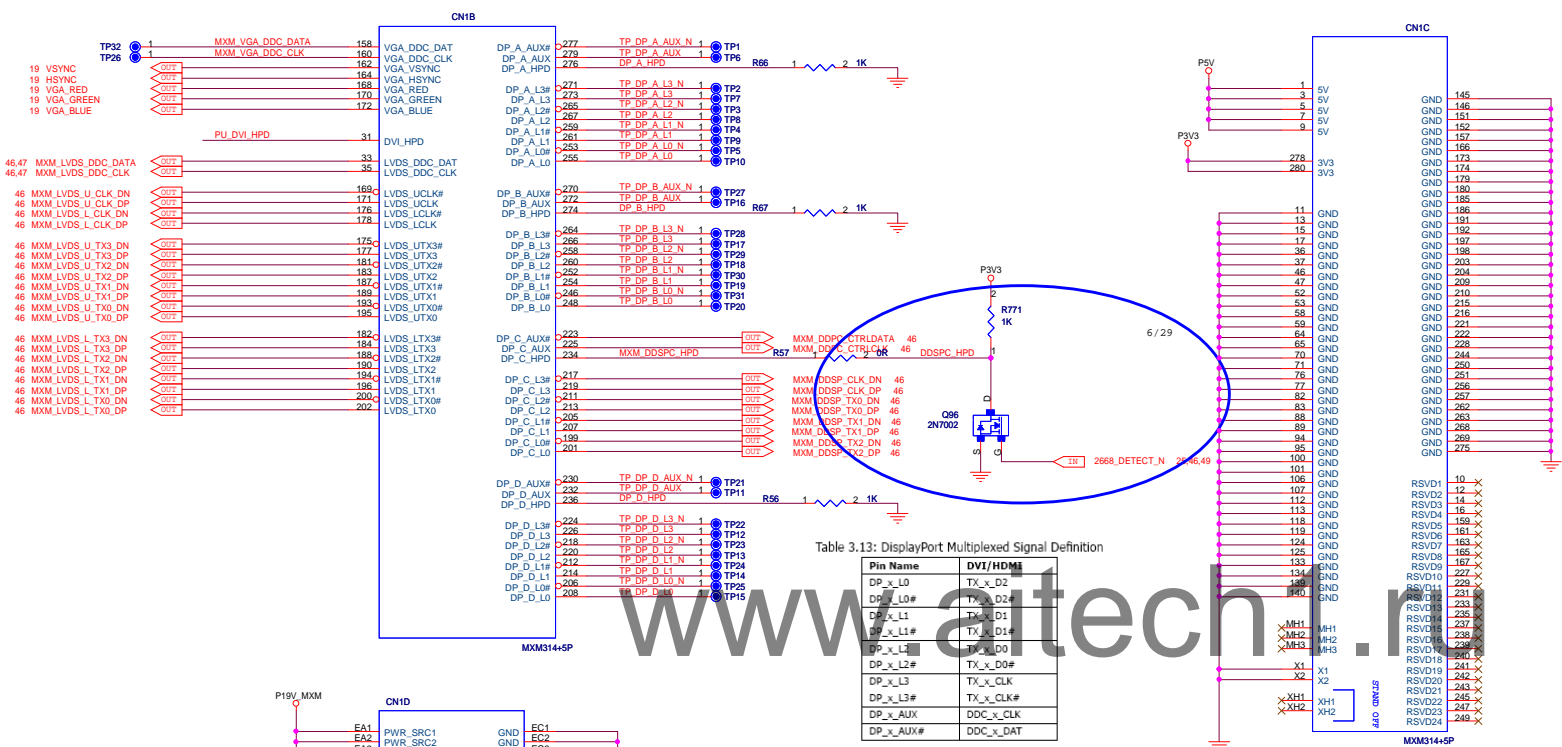
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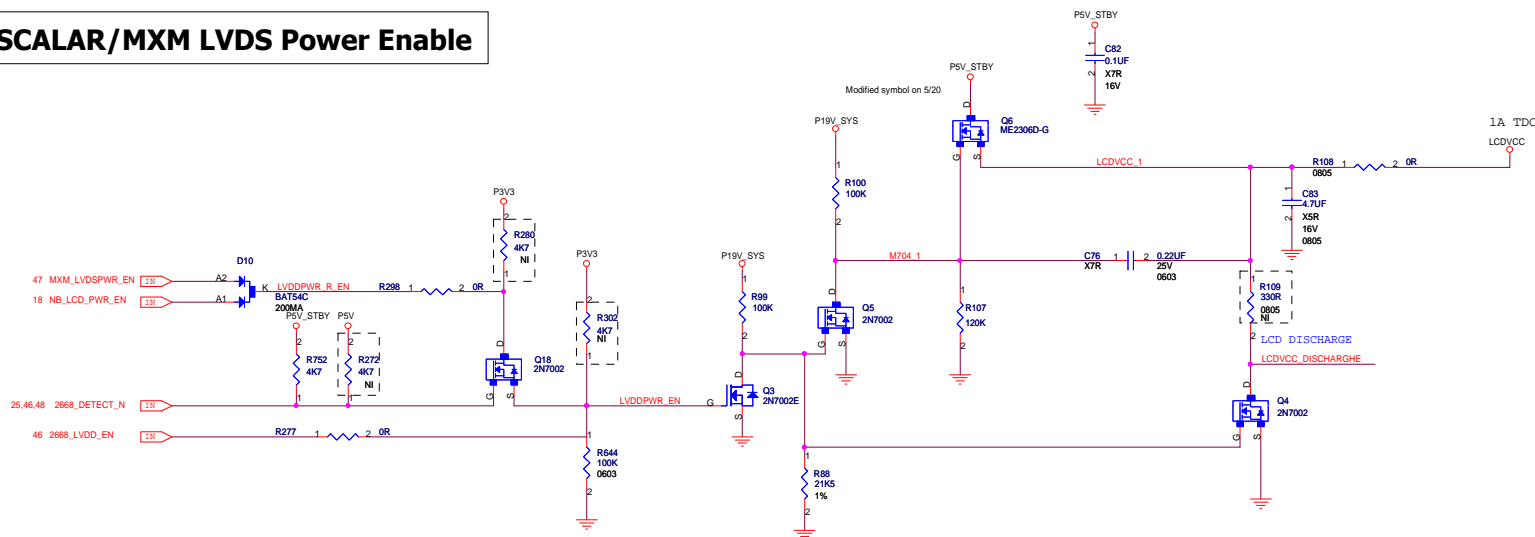
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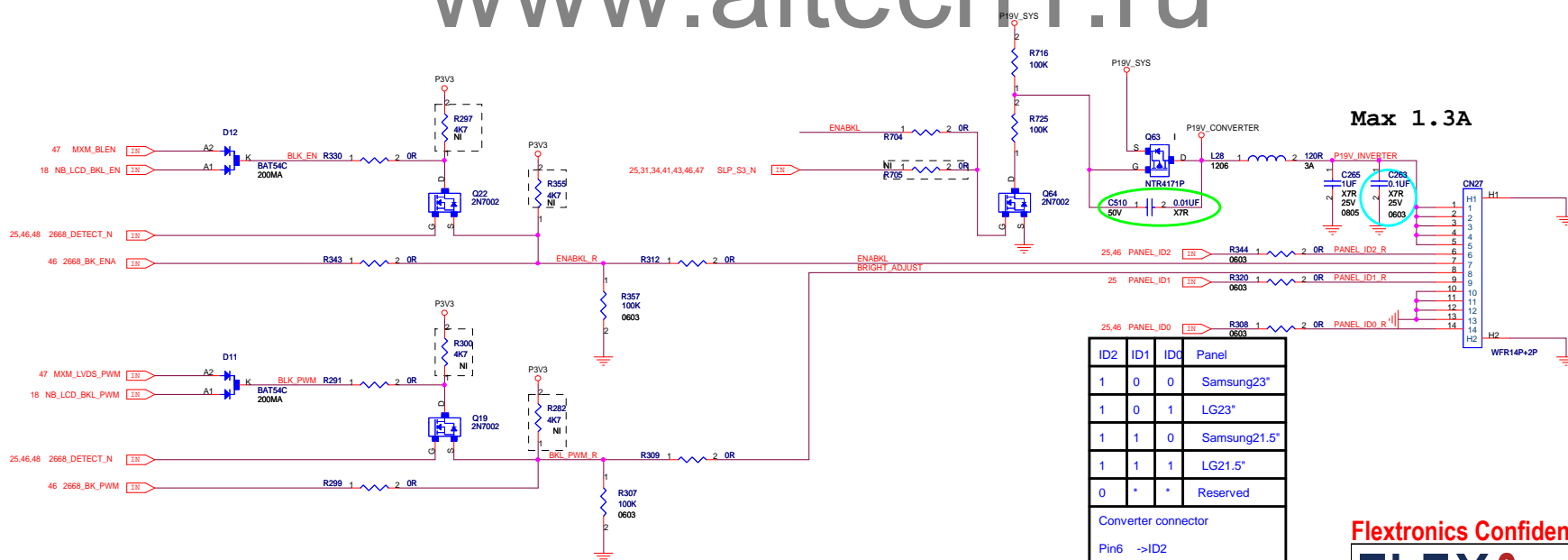




### SCALAR/MXM LVDS Power Enable

**CONVERTER CONN**

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ID2	ID1	ID0	Panel
1	0	0	Samsung23"
1	0	1	LG23"
1	1	0	Samsung21.5"
1	1	1	LG21.5"
0	*	*	Reserved

Converter connector

Pin6 -> I

Pin9 -> I

Pin14 ->II

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- X00\_0202y10
- 1.Page44 Delete M4,M6,M12,and add M7 By Kevin.
  - 2.Page10 R40 0 ohm change to insert.By Kevin
  - 3.Page29 R1850,R1851 change to NI,and R1853 change to insert,R1877 0 ohm change to insert.By Kevin
  - 4.Page32 R794 change to 10k,C479 change to 4.7uF,and R808 change to Insert.By Kevin
  - 5.Page32 R794 change to 10k,C479 change to 4.7uF,and R808 change to Insert.By Kevin
  - 6.Page10 R56.1net modified to CPU\_THERMDC\_R,and R57.1 net modified to CPU\_THERMDA\_R.By Kevin
  - 7.Page 30 R1907 39k2 change to 20k ohm 1%.By Kevin.
  - 8.Page 47 J29.1,J29.3,J29.5,J29.7,J29.9 net change to P5V\_MXM.By Kevin
  - 9.Page31 Add C1449,C1450 10uF,change R1919,R1920 tp 75 ohm,and add L44,L45 Bead,add R2100,R2101 22k. By Kevin.
  - 10.Page43 Add P5V\_STBY transfer to P5V\_MXM schematic. By Kevin
  - 11.Page49 Modified FAN schematic.By Kevin
  - 12.Page50. Modified Power Button and Ctrl volume schematic.By Kevin.

- X00\_0203y10
- 1.Page19 Add R231,R217,R232 150ohm.By Kevin.
  - 2.Page25 Net MXM\_PWR\_EN changes to GPIO55.
  3. Modified DRC Error.
  3. Page18 L4.2 net P1V8\_PLL change to P1V8,and delete R1997.

- X00\_0204y10
- 1.Page30 U16 ALC888-VC2-GR change to ALC888-VD2-GR.By Kevin.
  - 2.Page38 Delete PC150,151,152,153,154,158,160,161,163,164,166,168,and modified value PC145,146,147,148,149,155,156,157,159,162,165,167 to 22uF
  - 3.Page24 Delete R849,and R1939
  - 4.Page24 Add GPIO196 10k PU down.
  - 5.Page45 J6.31 GND change to P5V net. By Kevin.

- V01\_0308y10
1. Page 30 > Delete Q10 and R1921,R1896 4k7. Don't need MIC Bias voltage to add Line in channel
  2. Page 10 > VID[5:4] and VID[0] are unconnected PVIEN/VID[1] has a 300-ohm pulldown to VSS.For CPU Serial VID Mode
  3. Page 37 > Delete the net of CPU\_PVEN of PU resistor R2061,300R.For CPU Serial VID Mode
  4. Page 30 > U16.19 add C1452 4.7uF to GND.For For Scalar Audio decoupling
  5. Page 22 > EXT\_PCIE\_LAN\_CLKREQ\_N should connect to pin U46.4 CLKREQ3#.EXT\_MXM\_CLKREQ\_N should connect to pin U46.54 CLKREQ6#.For Clock Request Assign
  6. Page 8 > Delete R4,R5,J1,and R18,R19,R20,R21 1k ohm change to NI.Delete R8,R10,R11,R13,R14,R16 300 ohm,and R11,R12 300 ohm change to install.
  7. Page 10 > U1.F10,U1.E9,U1.D6,U1.E7,U1.F8,U1.C5,U1.AH9 change to connect TP.
  8. Page 19 > Delete cap C205,C206,and change L10.L11 to R145,R146 0 ohm 0603 to pull down VSS.
  9. Page 20 > Delete cap C264 1uF,and R139 pull down to VSS.Add PL68 connect to P1V1,but preserve to "NI".Add PL69 connect to P1V25.Delete C259,C260,C261,C262,C263,R138,and R140.
  10. Page 24 > R215 10k ohm change to NI.
  11. Page 25 > R270,R272 10k ohm change to NI.
  12. Page 26 > BIOS U10@BIOS change to M25PX32.Add U8.A8 connect to R2112 10k ohm to VSS.
  13. Page 27 > L21,L22,L23 change to MP-00006830-000.
  14. Page 29 > Add C150,C151 2.2uF 0603 for layout routing.
  15. Page 31 > EC21 update the symbol.
  16. Page 35 > add C102,C112,C117,C132 2.2uF 0603 for layout routing.The net of L51.1,L51.4 change opposite,and L51.2,L51.3 change opposite.L52.1,L52.4 change opposite ,and L52.2,L52.3 change opposite.
  17. Page 37 > PC6 1500pF change to "NI".PC8 22pF change to 100pF NPO 0603.PC12 1500pF change to "NI".
  18. Page 42 > Modified P1V1 sch.delete PQ12,PQ13,add PQ7.
  19. Page 44 > Add P1V25 schematic for NB enhance mode.
  20. Page 45 > stand off M1,M2,M3 change to MP-00008637-000
  21. Page 51 > delete Q46 ,R666,net LED\_SATA\_N connect to LED6.C,and R785.1 connect LED6.A,R785.2 connect to P3V3.

- V01\_0309y10
1. Page 29 > R615 change to install.Modified R1872,R1877,R1873 to 0 ohm.The net LAN\_ACT\_LED\_N connect to R1872.2,and EESK\_LED1 connect to R1873.2
  2. Page 25 > Delete R2010 ,and change net GPIO55 to BT\_DISABLE.
  3. Page 33 > Add R399 10k ohm PU to P3V3,and J20.51 connect to R1997.2,R1997.1 connect to BT\_DISABLE.
  4. Page 22 > U46.56 change to connect VSS by R189 0 ohm.
  5. Page 32 > Add R2113,R2114 0 ohm resistor.
  6. Page 32 > S3 change to MP-00008673-000.
  7. Page 25 > Add Board ID,and Panel ID schematic.
  8. Page 51 > Add PS2 KB/MS schematic.
  9. Page 51 > Add the net of 14M\_25M\_48M\_OSC ,and connect to R190.2
  10. Page 29 > reset pin (U12.25) connect to "PCIE\_RST\_N"
  11. Page 51 > Delete R685,Q55,and modified net PWR\_SLEEP\_LED\_N to PWR\_P5V\_STBY
  12. Page 13 > Modified Transistor Q80,Q81,Q82 pin E,C opposite.
  13. Page 13,14 > Update resistor R61,R62,R63,R64,R65,R66,R67,R68 100 ohm to 15 ohm valuse based on AMD suggest
  14. Page 37 > Updae the R2062 4K42 ohm to change to 1K ohm,base on AMD suggest. 3/10
  15. Page 8 > Delete R18,R19,R20,R20 pull up resistor,base on AMD suggest. 3/10
  16. Page 11 > Extra add PC158,C1453,C1454,C1455 to meet CPU\_VCORE decoupling requirement.By Kevin on 3/10
  17. Page 11 > Extra add C1456 to meet P1V2\_CPU\_VDDNB\_RUN decoupling requirement.By Kevin on 3/10
  18. Page 16 > Extra add C152 to meet CPU\_VCORE decoupling requirement.By Kevin on 3/10
  19. Page 40 > Add L99 for P2V5\_CPU\_VDDA\_RUN,base on AMD suggest.And add C684,C745 base Terry Suggest.
  20. Page 18 > R100 from 10k change to 4k7 ohm and add net SUS\_STAT\_N connect to R2121.
  21. Page 27 > L21,L22,L23 change to MP-00004404-000.
  22. Page 33 > R524 0 ohm change to "NI".That ensure LAN chip can work normal when install TV tuner card
- V01\_0312y10
1. Page 47 > R692 value from 4k7 change to 8k2,base on AMD\_GUAM sch.

- V01\_P007\_0315y10
1. Page 25 > Add Panel ID1 schematic
  1. Page 45 > Delete MH3
- V01\_P008\_0315y10
1. Page 51 > R585,R586,R588,R589 package change to 0402.
  2. Page 29 > Modified RTL8111E sch,include to delete EEPROM.And used strap pin in eFuse Function.
  3. Page 25 > R255 33 ohm change to 22 ohm 1%.

- V01\_P010\_0317y10
1. Page 22 > Modified clock generaotr to ICS9LPRS482

- V01\_P012\_0318y10
1. Page 45 > Modified Mount Hole spec.
  2. Page 22 > Modified clock generaotr to ICS9LRS4880
  3. Page 48 > MxM Slot change to MP-00009110-000
  4. Page 50 > Update the symbol for CIR Emitter ,touch panel ,CIR Receiver

- V01\_P014\_0319y10
1. Page 25 > Add net MXM Crad Detect ,and PU 2k2 to P3V3

- DELL\_X00\_P001\_0401y10
1. Page 30 > delete C431 1uF X5R
  2. Page 31 > delete EC22.EC23 100uF 7343,MP-00008964-000,remove R1914,R1915 22k MP-00005231-000 Replace C1449,C1450 4.7uF to change C1471,C1472 22uF/1206/16V R1919,R1920 1k change to 75 ohm.
  3. Page 51 > Add COM Port Function
  4. Page 25 > U8.D28 changeto connect to PWR\_P5V\_STBY
- DELL\_X00\_P002\_0407y10
1. Page 51 > LED6 MP-00000582-000 change to MP-00008667-000
  2. Page 35 > L48,L49,L50,L51,L52,L53 common choke change to MP-00008276-000
  3. Page 30 > net AUDIO\_MUTE(U11.47) connect to R144.1
  4. Page 38 > PC51,PC132 change to 10uF/X5R/25V/1206
  5. Page 30 > C419 change to MP-00004054-000
  6. Page 35 > J23,J43,J44,J45 from MP-00008629-000 to MP-00009248-000,and J25,J26 side USB CONN from MP-00008628-000 to MP-00008627-000
  7. Page 33 > J16,J17 from MP-00003525-000 to MP-00003522-000 to solve the problem, it is short pin connector
  8. Page 51 > LED4 from MP-00004434-000 to MP-00003873-000 to solve the problem
  9. Page 51 > EC20 MP-00008519-000 need move and avoid MiniPCIe interfere
  10. Page 24,25 > JP3.JP7,JP8,JP9,JP10,J12 change to MP-00007256-000 pinch 2.0mm

- DELL\_X00\_P003\_0412y10
1. Page 31 > R1822 change to NI ,and delete D33.
  2. Page 25 > Delete JP9,JP10,JP11,J104,J108,R2120,R2127,R2140 for Panel ID select
  3. Page 49 > add R2181,R2184,R2185 0 ohm 0603 resistor.
  4. Page 50 > Delete R544,R544,C459,R444,R466,R469,R494,Q31,Q82
  5. Page 47 > Delete R672,R673 0 ohm resistor.And delete net MXM\_SDATA\_R,MXM\_SCLK\_R.
  6. Page 34 > R1831 change to insert.Add net SIO\_SMB\_CLK pull-up R1838 10k to P3V3\_STBY,net SIO\_SMB\_DATA pull-up to R1839 10k to P3V3\_STBY.
  7. Page 33 > Delete net PCIE\_TUNER\_CLKREQ\_N and R1885,and delete net PCIE\_WLAN\_CLKREQ\_N,R1887 0 ohm.
  8. Page 47 > Delete net MXM\_CLKREQ\_N and R1890,R692 change to NI.
  9. Page 22 > Clock generator change to ICS9LPRS482

- DELL\_X00\_P004\_0415y10
1. Page 32 > Delete C482 and add PC90 220uF for P3V3 rising time request.
  2. Page 51 > R2182,R2183 change to 0 ohm 0603,and R573 change to 330R 0805, and R571,R572 change to 330R 0805
  3. Page 32 > PC90 change to EC21
  4. Page 19 > R118 change to MP-00001736-000
  5. Page 22 > Add C276,C279,C280,C281,C282,C284 0.1uF.Modified the CLK assign routing.
  6. Page 47 > R676 8k2 change to 10k and keep NI.And add TP150,TP144,TP148,TP149.
  7. Page 43 > Delete P5V\_MXM schematic
  8. Page 46 > Add R2176 0 ohm 0603
  9. Page 49 > R613 change to NI.
  10. Page 33 > J16,J17 change to MP-00008098-000
  11. Page 29 > Add PE\_WAKE\_NIC\_N PU 10k to AVDD33\_LAN,but resistor keep NI.And R616 0 ohm change to 220R.
  12. Page 35 > C376,C379,C381,C383,C525,C527 100uF change to MP-00007298-000
  13. Page 50 > R2150 change to NI,Q64,Q618,R2148,C532 change to insert.
  14. Page 30 > Add P5V\_USB to P5V\_AUDIO\_AVDD for Energy star 5.0 solution, check it on EVT duild
  15. Page 34 > SIO\_RSMRST\_N PU 10k to P3V3\_STBY,but resistor keep NI.And R918 change to NI.
  16. Page 51 > Change power button breathe schematic

- DELL\_X00\_P005\_0419y10
1. Page 46 > Add R2174 0 ohm 0603 ,Pin J106.42 P5V\_STBY change to GND.Add C1476,C1477,C1478,C1479 10pF ,but keep "NI" for EMI fine tune
  2. Page 48 > Pin J29C.1,2,3,4,5 P5V\_MXM change to P5V,add C1473,C1474 10pF ,but keep "NI"for EMI fine tune.
  3. Page 33 > Add C1480,C1481,C1482,C1483,C1484,C1485 10pF 50V,but keep "NI" for EMI fine tune.
- DELL\_X00\_P007\_0420y10
1. Page 41 > Add PC244,PC248 POLYMER,6.3X6,560UF,2V5,20% close to PL42
  2. Page 33 > Add R1997 0 ohm ,but keep "NI".Delete TP352
  3. Page 40 > R2093, R2096 change from 1k to 20K,C643, C677 change from 0.1uF to 1uF,R2043 change from 5K to 20K,R452 change from 5K to 10K
  - 5.23K,U36,U64 VIN from P3V3 change to P1V5\_CPU\_VDDIO\_SUS
  4. Page 11 > R1993 change from 0 ohm to NI
  5. Page 43 > Change C519 for 0.1uF to NI

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